A 1.8V 2nd-Order ΣΔ Modulator

by

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Abstract

Low-voltage, low-power analog-to-digital converters provide a critical interface in portable mixed-signal electronic systems. The robustness and tolerance of the sigma-delta modulator technique over other data-converter techniques make it an ideal choice in applications where low voltage and high-dynamic range are a must.

This thesis deals with the design and implementation of a low-voltage, low-power 2nd-order sigma-delta modulator with a single 1.8 V power supply using conventional threshold voltage transistors. All the circuit blocks are integrated on one chip, and the input common-mode voltage is set at mid-rail, resulting in low power dissipation, minimum off-chip components, and high efficiency, flexibility and compatibility. The design is useful for voice applications in personal communications systems supplied by two nickel-cadmium or alkaline batteries.

The modulator consists of four circuit blocks: the biasing, the operational amplifier, the comparator-latch, and the four-phase clock generator. A high DC gain, large output swing operational amplifier with a low-voltage power supply was implemented using a fully-differential folded-cascode input stage followed by a common-source output stage, combined with a switched-capacitor common-mode feedback circuit. Based on fully-differential switched-capacitor techniques, the modulator was implemented using a 3.3 V, double-poly, 0.35μm CMOS process. The modulator exhibits a 15-bit dynamic range for a 7 kHz bandwidth, and a 14-bit dynamic range for a 20 kHz bandwidth at an oversampling frequency of 2.56 MHz. The complete 2nd-order modulator has a power dissipation of 0.99 mW, and occupies 0.31 mm^2 of die area excluding bonding pads.

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CHAPTER 1

Introduction

1.1 Purpose and Motivation

Analog-to-digital converters provide an irreplaceable link between the analog world of transducers and the digital world of signal processing systems. As the key components in modern electronic systems used to translate an analog signal to a digital representation, they can facilitate the processing of the data in a digital environment. Developments in VLSI digital IC technologies have made it attractive to perform many signal processing functions in the digital domain placing even more importance on analog to digital converters that can be integrated in fabrication technologies optimized for digital circuits and systems [1, 2].

The process of converting an analog signal to a digital one often limits the speed and resolution of the overall system. As a result, traditional research efforts have been focussed on developing A/D converters that achieve both high speed and high resolution [3]. Nowadays, with the explosive growth in the demand for portable, battery-operated electronics for communications, computing, and consumer applications, as well as the continued scaling-down of VLSI technology, the focus has been on the design of integrated A/D converters for portable devices featuring low power dissipation, low cost, and high reliability [4, 5].

High levels of integration not only result in reduced cost and increased reliability, but also reduce the need for the constituent analog and mixed-signal circuit blocks to drive large

pad and package parasitic capacitances, thereby conserving power [6]. Lower power supply voltages not only minimize the number of batteries, thus reducing both size and weight, but also result in significant power saving in digital circuits. Although in analog circuits, lower power supply voltage does not necessary imply low power dissipation due to the need to keep the same dynamic range, it is still possible and desirable to realize low-power analog circuits at low voltages with appropriate circuit architectures and process technologies [7].

The primary aim of this project is to design a low power, low voltage, high dynamic range A/D converter for voice band communication applications using a 3.3 V, 0.35μm CMOS technology, but operating at 1.8V.

1.2 Analog-to-digital Converter Architectures

The analog-to-digital conversion of a signal includes two basic operations: uniform sampling in time, and quantization in amplitude. The sampling process creates periodically repeated versions of the signal spectrum at multiples of the sampling frequency, while the quantization process translates the sampled signal amplitude to a finite set of output values that are represented by a digital code word composed of a finite number of bits. These digital code words are often said to be in pulse-code-modulation (PCM) format. Although analog-to-digital converters can be implemented in a variety of architectures, trading off speed, resolution and circuit complexity, they are all basically categorized into two main types: Nyquist-rate converters and over-sampling converters [8, 9].

1.2.1 Nyquist-rate ADC

In Nyquist-rate converters the sampling frequency equals the signal Nyquist rate, i.e. twice the input signal bandwidth. When used in conventional mode, as illustrated in Figure 1.1, a low-pass analog filter is needed to attenuate high frequency noise and out-of-band components that alias into the input signal. The three basic types of the Nyquist-rate converter are: the parallel, the serial and the subranging converter.

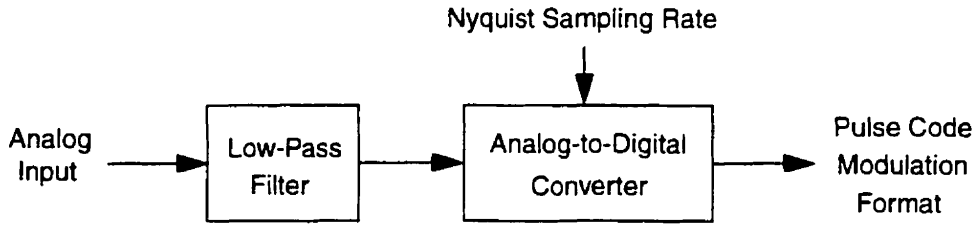

Fig. 1.1: Conventional Nyquist-rate ADC

I. Parallel ADC

The parallel A/D architecture, commonly referred to as flash A/D converter, provides the fastest possible approach to quantizing an analog signal. In a N-bit flash converter, shown in Figure 1.2, all digital bits are converted simultaneously by 2^N-1 voltage comparators with a set of reference voltages generated by a resistor divider, followed by a priority encoder that converts the comparator outputs to binary information.

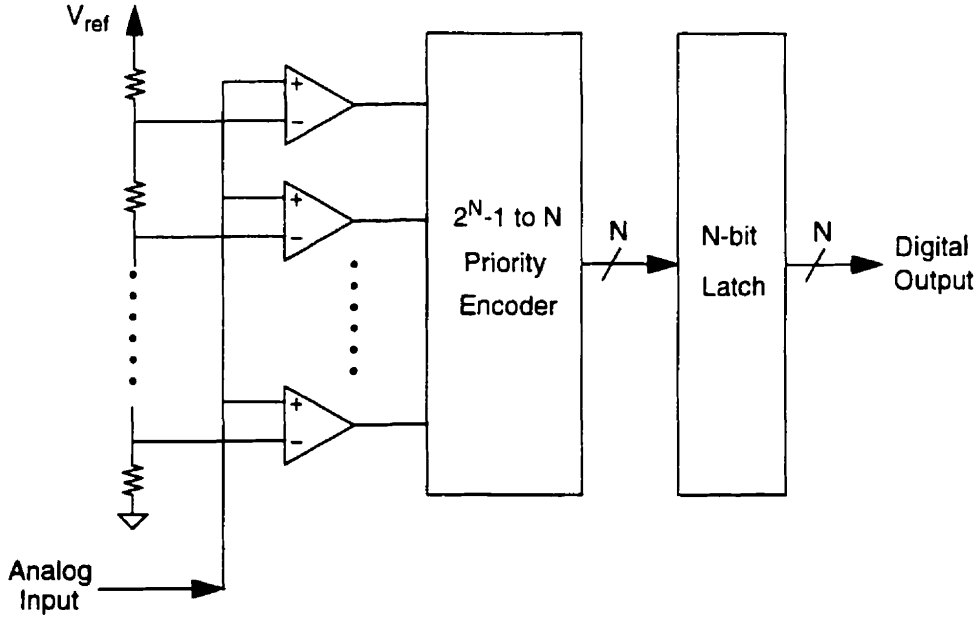

Fig. 1.2: Parallel ADC Architecture

The parallel architecture has the highest conversion speed but usually consumes significant power and large die area that increases exponentially as the number of bits

increases. Typically no more than 10 bits resolution can be obtained without component trimming and excessive area consumption [4]. Parallel converters have been implemented most commonly in bipolar technology because of the excellent V_{BE} matching that allows comparator design accurate to eight bits or more.

II. Serial ADC

In serial converters, each bit is converted in sequence, one at a time. These converters are relatively slow compared to the parallel ones but the lack of speed is made up by low cost, ease of construction and high resolution. The three main architectures are the successive-approximation, the algorithmic, and the integrating converters.

Successive-Approximation ADC

Successive-approximation converters are the most widely implemented serial ADCs. In the basic architecture, shown in Figure 1.3, the converter uses a binary search algorithm to determine the closest digital output generated by the successive-approximation register latch to match an input signal.

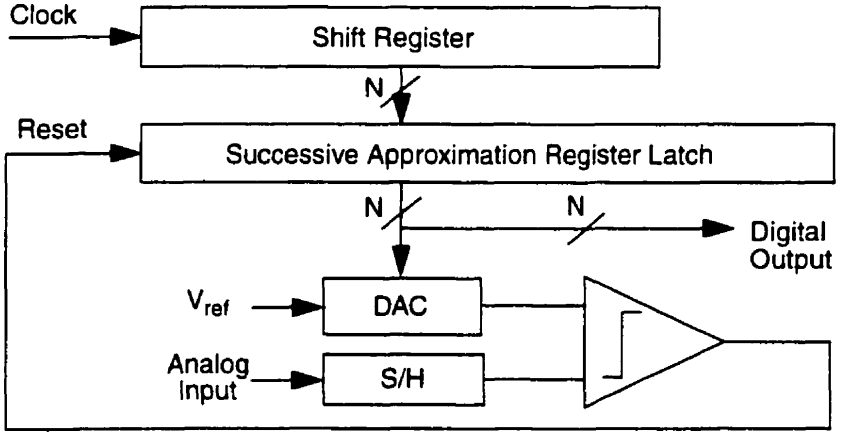

Fig. 1.3: Successive-Approximation ADC Architecture

With the shift register enabling one bit at a time, each approximation cycle generates a one-bit conversion result, thus N clock cycles are needed to complete an N-bit conversion.

A precisely controlled reference signal is needed to be generated by a DAC in each clock cycle and a sample-and-hold circuit is needed to keep the input signal stable while each bit is evaluated. The DAC limits the ADC linearity and consumes significant power and area. This converter exhibits a wide range of conversion speed and 8 to 16 bits of resolution.

Algorithmic ADC

The algorithmic converter is a serial converter that operates in much the same way as the successive-approximation converter. However, unlike a successive-approximation converter which adjusts the reference voltage in each cycle, an algorithmic converter doubles the feedback voltage while leaving the reference voltage unchanged.

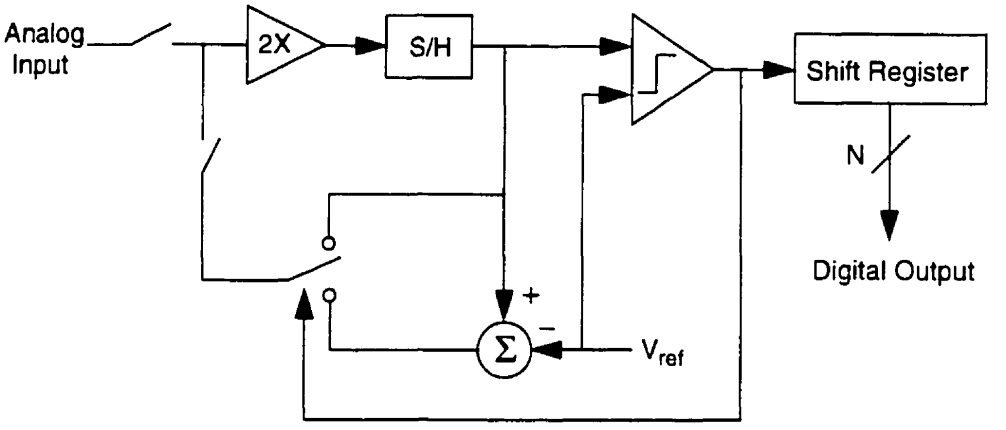

Fig. 1.4: Algorithmic ADC Architecture

As shown in Figure 1.4, after the analog input signal is stored in the S/H with a gain of 2, it is not only compared with the reference signal to resolve the MSB, but also fed back to the input at the same time. The comparison result determines whether this feed back signal is to be subtracted by the reference voltage, and a new comparison is then performed to realize the next bit conversion. This converter eliminates the need for the DAC, and thus dissipates less power, occupies less area with a simple architecture and small components. The identical comparison stage for each bit also results in improved linearity, but the accuracy of the multiplier is the limiting factor in achieving a high resolution.

Integrating ADC

The integrating converter is the third kind of serial ADC, which is dominantly used in high-accuracy, very low speed signal conversion.

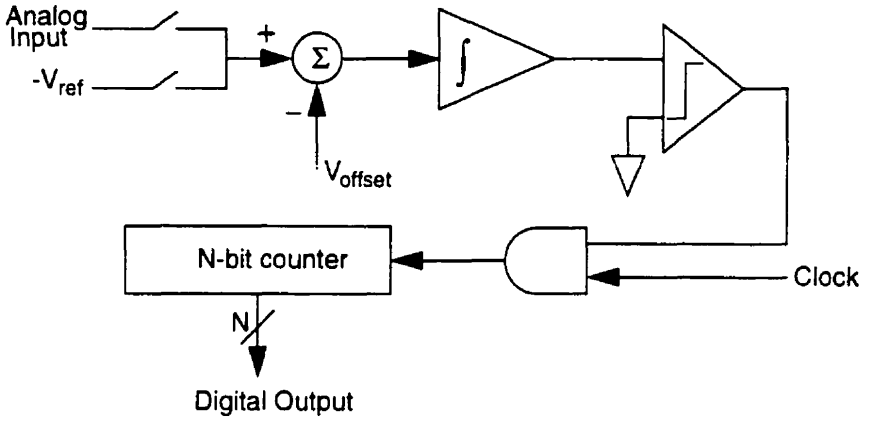

Fig. 1.5: Integrating ADC Architecture

Using the architecture shown in Figure 1.5, the quantization of an analog input signal is realized in three steps: auto-zero operating by the offset voltage, charging the integrator's capacitor with the input signal for 2^N clock cycle time, and discharging the same capacitor by a current sink generated by the reference voltage. With the final digital output generated by the N-bit counter, a full-scale signal conversion needs 2^{N+1} clock cycle time to complete if the auto-zeroing time is neglected. Although the accuracy of the digital counter and the linearity of current sink are the limitations, its relatively low offset, low gain errors and high linearity are the advantages in addition to the small amount of circuitry required in implementation. These converters are traditionally used for voltage and current meter applications.

III. Subranging ADC

The subranging converter, also called the hybrid converter because of its combination of both serial and parallel architectures, has the advantages of both approaches. In a two-stage subranging architecture shown in Figure 1.6, the first flash ADC generates the first

N/2 MSBs while the second flash ADC determines the remaining N/2 LSBs by detecting the quantization error generated by the first stage. A typical example of the subranging converter is the pipelined converter in which the stage number is increased to N, and each stage resolves a single bit. It has the advantage of inherent single-path sampling of the signal, which gives good high-frequency effective bit performance, and the capability of using non-critical purely dynamic comparators [10].

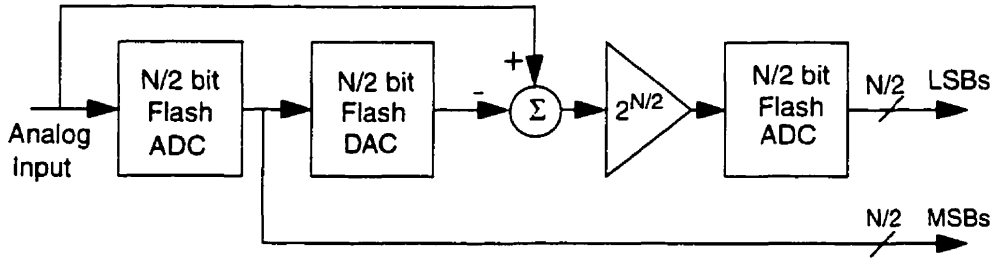

Fig. 1.6: Subranging ADC Architecture

Although it takes N clock cycles to process each signal, a new sample can be entered in the pipeline during each clock cycle, thus making the processing rate still one sample per cycle. The pipelined converter is more popular than the flash converter for high-speed, medium-accuracy data conversion due to its advantages such as small silicon area, low power dissipation, low load capacitance, and low stringent comparator resolution. The limitation of subranging converters is the error generated by the DAC. Digital error correction is commonly needed to ease the accuracy requirement.

Basically, high resolution Nyquist-rate converters require precise analog components in filters and conversion circuits. They are often difficult to implement in sub-micron VLSI technology because they are very vulnerable to noise and interference. The resolution of such converters is limited by the technology used in the implementation, and the anti-aliasing filters must have a sharp cutoff frequency [11]. However, oversampling converters can use simple analog components to achieve a high resolution, but they require complex digital signal processing stages.

1.2.2 Oversampling ADC

An oversampling converter has a sampling clock frequency that is much higher than the input signal's Nyquist rate. It typically consists of a modulator and a decimation filter in an oversampling conversion mode, as shown in Figure 1.7. First, the analog signal is pulse density modulated through the modulator into a simple code, usually a single-bit word, output which is then smoothed by a decimation filter. Noise, interference, and high-frequency signals are attenuated before aliasing into the signal band when the code is later re-sampled at the Nyquist rate.

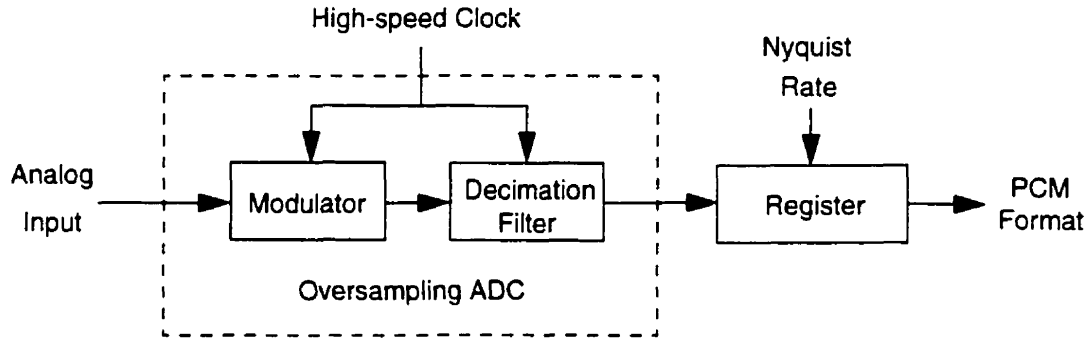

Fig. 1.7: Oversampling ADC

The design of the modulator trades resolution in time for resolution in amplitude so that imprecise analog circuits can be used [12, 13]. This trade-off between relaxed analog circuitry requirements and complicated digital circuitry is desirable because of the rapid advancement of modern VLSI technologies, which are better suited for fast digital circuits than precise analog ones. With their sampling rate several orders higher than the Nyquist rate, oversampling converters make extensive use of digital signal processing and may eliminate the need for both an analog anti-aliasing filter and a sample and hold cell at the input of the ADC. Shaping the quantization noise through the use of feedback is often used to achieve a converter resolution up to 20 bits [3, 8, 9]. Figure 1.8 shows the architecture of an oversampling ΣΔ modulator that consists of a series of integrators and a quantizer in a feedback loop. The number of integrators determines the order of a ΣΔ modulator, and the

sampling rate to its Nyquist rate defines the oversampling ratio [14]. The feedback loop spectrally shapes the quantization noise by attenuating the quantization noise at low frequency while emphasizing the high frequency noise which can be shifted out of the signal band by means of a digital low-pass filter operating on the output of the ΣΔ modulator [1, 15]. In Figure 1.8, each integrator's input is the difference between the previous integrator's output and the D/A converter's output. The effect of the feedback loop is to bring the average value at the first integrator input to zero. This implies that the output of the D/A converter is on average equal to the input signal X(Z). So the Y(Z) is on average equal to X(Z). The degree to which the quantization noise can be attenuated depends on the order of noise shaping employed and the oversampling ratio [15].

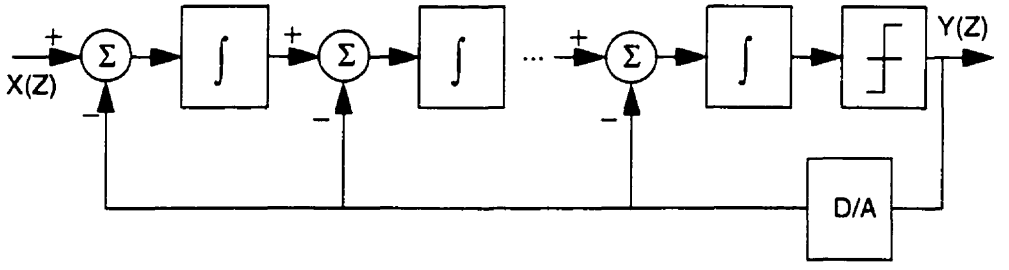

Fig. 1.8: Sigma-Delta ADC Architecture

Basically there are three categories of oversampling modulators: noise-shaping, predictive, and predictive/noise-shaping modulators. The noise-shaping modulator has important practical advantages in terms of insensitivity to the imperfections in the analog circuitry [16].

Oversampling architectures are suitable for relatively low-frequency applications such as digital audio, digital telephony and instrumentation. They are often implemented in a CMOS process, which allows the signal processing blocks to be constructed using switched-capacitor sampled-data techniques. Along with the simple structure, they are very suitable for low-power, low-voltage design.

1.2.3 Comparison of ADC

The conversion speed of the various ADCs discussed above can be compared qualitatively by using the concept of "analog clock cycles" [10].

Figure 1.9 shows the clock cycle needed per output sample as a function of the resolution for various ADCs. One analog clock cycle involves one analog operation such as comparison, D/A converter settling, and operational amplifier settling. Although one clock cycle time is both technology and implementation dependent, the number of cycles required for producing one effective quantized output sample does not change. As shown in Figure 1.9, the parallel and subranging converters need only one clock cycle, regardless of resolution. The others require more clock cycles which are proportional to the resolution. The clock cycles needed for each output sample determine the conversion speed, and the ADC operating bandwidth.

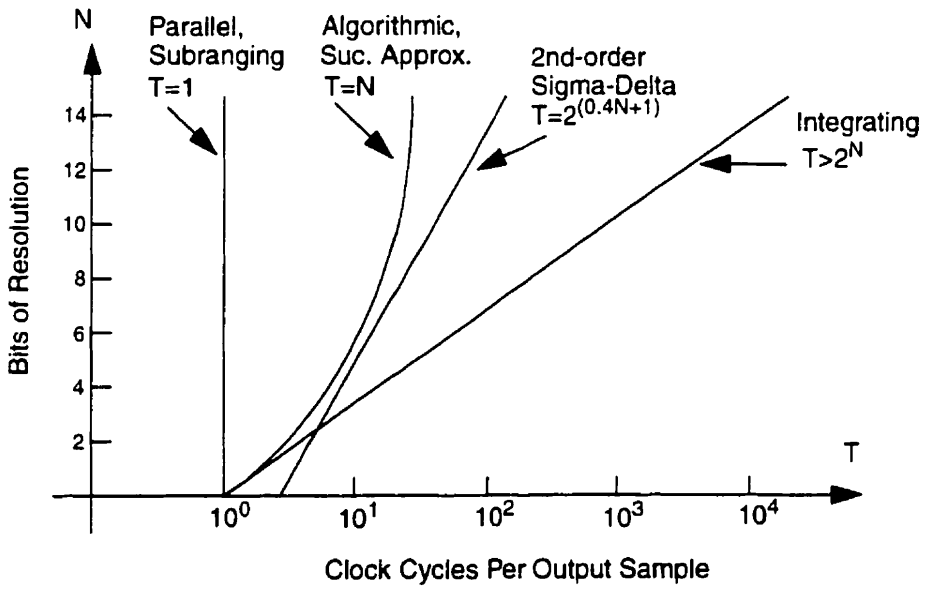

Fig. 1.9: Comparison of ADC's Conversion Speed

The conversion speed and maximum resolution trade-off that an ADC can achieve is qualitatively described in Figure 1.10. The sigma-delta ADC can achieve the highest resolution for relatively low conversion speed, and is ideally suited for speech applications.

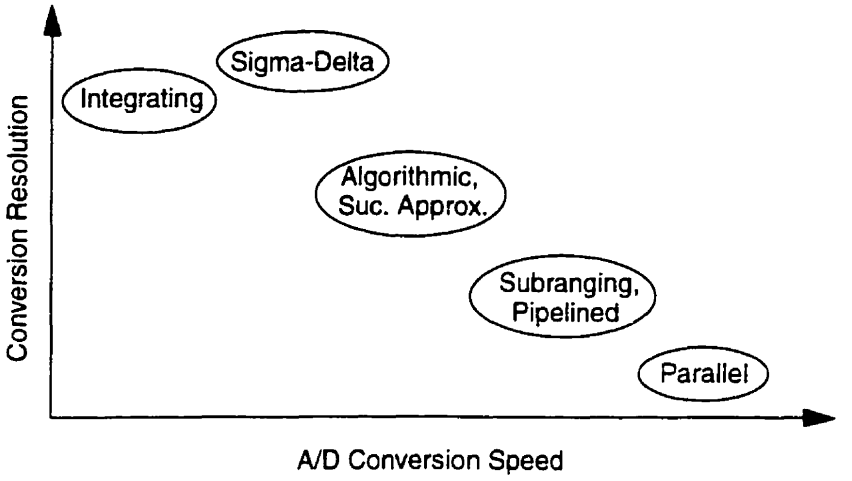

Fig. 1.10: Trading Conversion Speed for Resolution

1.3 Sigma-Delta Modulators

1.3.1 Distinguishing Features

As mentioned previously, in addition to the reduced requirement on the number, precision and complexity of analog circuits, which is important under low-voltage supplies, the ΣΔ modulator offers many other distinguishing features.

The dynamic range of a ΣΔ modulator can be increased by increasing the oversampling ratio (*OSR*) and the order of the feedback loop [14]. Modifying the *OSR* does not influence the circuit itself while increasing the order simply means adding another integrator but still keeping the same circuit configuration. Also since the conversion rate can be traded off directly for resolution through digital decimation, the converter specifications can be directly customized for the required application without changing the analog circuitry [12, 17, 18]. Furthermore, because digital decimation can be treated as part of the overall signal processing requirements for the whole system, it results in both cost and performance advantages for the end user. In this way, oversampling converters not only perform quantization like conventional ADCs, but also act as a complete signal-acquisition interface [19].

The ΣΔ modulator simplifies the requirement placed on the analog anti-aliasing filter because of the high rate of oversampling. A continuous-time anti-aliasing filter for an oversampling converter is still necessary, but only for anti-aliasing protection against the high initial sampling rate. The large difference between the desired signal bandwidth and the new anti-aliasing cut-off frequency means that the available transition bandwidth for the filter is many times its passband width, and this makes it much easier to realize the anti-aliasing filter with low precision analog circuitry. The oversampled signal must be further filtered to suppress frequencies higher than half of the Nyquist frequency, but this occurs digitally after the signal has been quantized [4, 19].

By using single-bit quantization within the feedback loop, a ΣΔ modulator yields low distortion and high linearity conversion in that an in-loop 1-bit DAC only has two output values. Since two points define a straight line, no trimming or calibration is required for the 1-bit DAC [8, 20]. Along with the oversampling rates, a ΣΔ modulator greatly improves the ADC's resolution on the accuracy available from circuit element matching in a Nyquist-rate converter [21].

The ΣΔ modulator offers a power-efficient way of implementing a high-resolution A/D converter because much of the signal processing occurs in the digital domain where power consumption can be dramatically reduced simply by scaling the technology and reducing the voltage supply [1, 7, 22]. The relaxed requirements for the analog anti-aliasing filter also represent a significant power dissipation advantage in comparison with Nyquist-rate converters [5, 23].

By oversampling and noise-shaping, the ΣΔ modulator is more robust against circuit imperfections than conventional quantizers because the signal binary quantizer is less sensitive to circuit mismatch and precision [19, 24].

Although the digital signal processing stage is an expense associated with using a ΣΔ modulator, the dramatic down-scaling of digital circuits coupled with the optimized design of infinite impulse response (IIR) filters can result in greatly reduced die area for decimating and interpolating filters [25].

However, some problems remain when implementing a ΣΔ converter. The quantization noise is actually signal dependent and not statistically uncorrelated as is usually assumed. This results in reduced performance, especially in low-order modulators. High-order ΣΔ modulators make the quantization noise less signal dependent and cause higher effective resolution to be achieved for the same oversampling ratio, but they suffer from instability problems [24]. A higher oversampling ratio leads to a higher resolution, but results in more power consumption [22]. Compared with the parallel architectures, the ΣΔ modulator also has a limited bandwidth due to oversampling.

All these features make the ΣΔ modulator appealing for high-resolution, relatively low-frequency audio applications [17, 26].

1.3.2 Architecture Trade-offs

For a range of applications, a variety of ΣΔ modulator architectures have been suggested, which can be classified as either single-loop or multi-stage types [9, 23, 27]. The single-loop uses one quantizer and a D/A converter along with a series of integrators while the multi-stage consists of a cascade of single-loop ΣΔ modulators. Both architectures can employ either single-bit or multi-bit quantizers and combined D/A converters [14]. High order single-loop architectures suffer from potential instability owing to the accumulation of large signals in the integrators [1, 28]. Cascade architectures use combinations of inherently stable low order single loops to achieve higher order noise-shaping, but the constraints on circuit imperfection and mismatch will be more severe [1, 14, 20]. Combining multi-bit D/A converters results in reduced quantization noise, improved

dynamic range, de-correlated quantization noise spectrum for the input signal, and improved stability [28-30], but the multi-bit DAC cannot be easily fabricated in VLSI technology with the linearity needed for high resolution conversion. Furthermore, the multi-bit output also complicates the digital low-pass filter following the modulator [11, 14, 31].

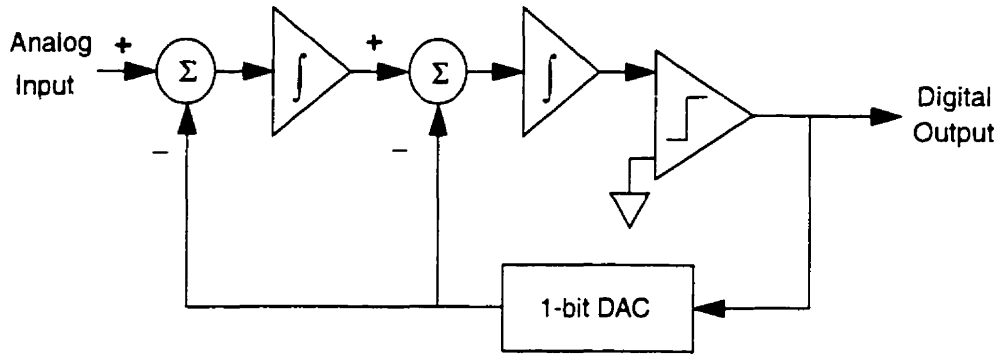

Fig. 1.11: Second-Order Sigma-Delta ADC Architecture

The trade-offs between resolution, bandwidth, circuit complexity and modulator stability, make second-order ΣΔ modulators shown in Figure 1.11 particularly attractive for high resolution A/D conversion [11]. The effectiveness of second-order ΣΔ modulator architectures has already been illustrated in a variety of applications, and the extension of performance achievable with such architectures to the levels required for audio and higher signal bandwidths has been demonstrated [1].

A ΣΔ modulator can be implemented by designing the loop integrator either in the discrete-time domain such as switched-capacitor filters [32] or in the continuous-time domain such as with RC [33], transconductor [34] and LC [35] filters. Continuous-time modulators are much faster and provide a certain amount of antialias filtering, but they are more sensitive to clock phase noise because clock jitter modulates both noise and signal powers in continuous-time loops. High-speed continuous-time circuits typically have poorer linearity than switched-capacitor circuits in which the amplifiers are linearized by feedback

and pulse shapes during settling have no effect on the final output [36]. At present, most reported ΣΔ modulators are implemented using switched-capacitor techniques [36, 37].

1.4 Previous Work on Low-Voltage ΣΔ Modulator

Table 1.1: Recent Work on Low Voltage ΣΔ Modulator

Specifications	Ma [17] 1998	Au [22] 1997	Rabii [5] 1997	Zwan [38] 1996	Grilo [39] 1996
Order of ΣΔ	2nd	3rd	3rd	4th	2nd
Power Supply	1V	1.95V	1.8V	2.2V	1.8V
Power Consumption	425μW	340 μW	2.5mW	0.2mW	2mW
Dynamic Range	14bits	12bits	16bits	13bits	15bits
SNDR	-	11bits	15bits	12bits	13bits
Sampling Frequency	2MHz	1MHz	4MHz	512kHz	2MHz
Bandwidth	7kHz	8kHz	25kHz	3.4kHz	3.5kHz
Technology	0.5μm CMOS	1.2μm CMOS	0.8μm CMOS	0.5μm CMOS	0.6μm CMOS

The recent work on low-voltage ΣΔ modulators is summarized in Table 1.1. Of these reported modulators, two are of particular relevance. Ma's design [17] was realized in a CMOS process optimized for low-voltage applications (threshold voltage 0.3 V) which is not commonly available. Grilo's work [39], while implemented on a conventional digital process (threshold voltage 0.7 V), has a relatively low bandwidth (3.5 kHz) and high power dissipation.

1.5 Thesis Objective

The objective of this thesis is to implement a low-power second-order ΣΔ modulator for digital hearing aid products, with the latest CMOS fabrication technology conventionally optimized for digital circuits and systems.

The TSMC 3.3 V, 0.35μm CMOS technology is used for the implementation. With a threshold voltage around 0.7 V, a single 1.8 V power supply voltage is used to make the design suitable for electronic systems supplied by two nickel-cadmium or alkaline cell batteries in series, while achieving a dynamic range of 15 bits, an input bandwidth of 8 kHz, and a power dissipation less than 1 milliwatt.

Unlike most of the previous low-voltage reported designs, this design is intended to include all the circuit elements on a single chip. The chip pins are only dedicated for the power supply, clock signal, analog inputs and digital outputs. Input common-mode voltage is assumed to be halfway between the power-supply voltages instead of analog ground in such a way to provide an easier interface with other IC components. As a result, the power dissipation is minimum, the number of off-chip components is dramatically reduced, and the efficiency, flexibility and compatibility of the circuit are improved.

Chapter 2 discusses the theory and design concepts of a second-order ΣΔ modulator. Not only the oversampling and noise-shaping theory are explained and demonstrated by high-level simulation techniques, but also the key design principles and trade-off considerations are described in detail. All the building blocks' specifications, including the integrator cell design requirements, are discussed.

Chapter 3 presents the transistor level design of the building blocks including the biasing, the operational-amplifier, the comparator and the clock generator. Circuit, simulation results and layout implementation of each block are discussed as well as the final realization of the second order ΣΔ modulator. Test results of the final experimental implementation are also reported.

Chapter 4 provides conclusions and suggestions for future work.

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CHAPTER 2

Second-Order Sigma-Delta Modulator

2.1 Introduction

The standard architecture of a second-order ΣΔ modulator includes two integrators, one quantizer and one D/A converter, which are embedded within a feedback loop as shown in Figure 2.1 [1, 2].

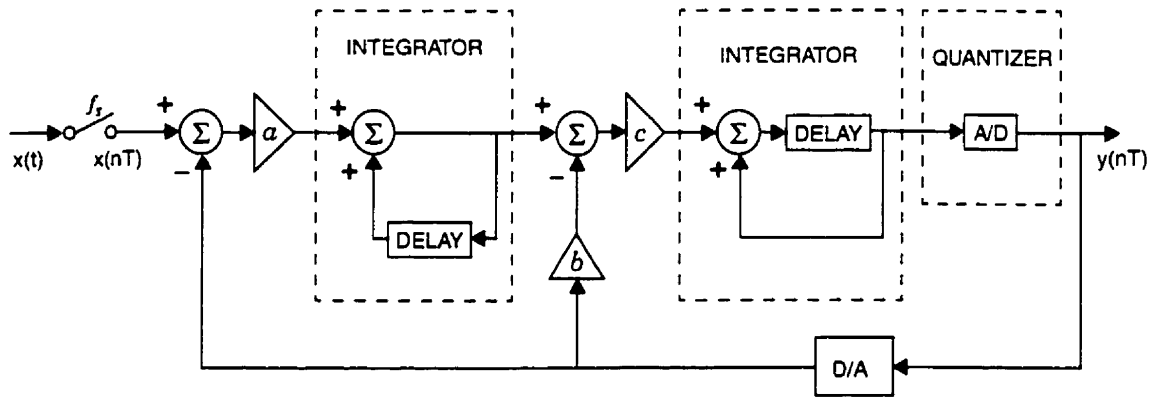

Fig. 2.1: Second-Order Sigma-Delta Modulator Diagram

An analog input signal *x(t)* is sampled at a high frequency f_s, and a high-speed low-resolution digital signal *y(nT)* is generated at the output that is further processed in the digital domain to produce a Nyquist-rate high-resolution digital output [1, 2]. This efficient method of trading off speed for resolution in a ΣΔ modulator technique is based on two concepts: oversampling and noise-shaping [3].

2.2 Oversampling and Noise-Shaping

Oversampling reduces the quantization noise power in the signal band by spreading a fixed quantization noise power over a bandwidth that is much larger than the signal band, while noise-shaping further attenuates this noise in the signal band and amplifies it outside the signal band [3, 4, 5].

2.2.1 Oversampling

Oversampling theory is based on an exact quantization model that the output quantized signal $y(n)$ is the sum of the input signal value $x(n)$ and the quantization error $e(n)$, which is strongly related to the input signal. For a rapidly and randomly active input signal $x(n)$, $e(n)$ can be assumed to be a statistically uncorrelated white-noise signal, leading to an approximate quantizer model with reasonably accurate results [6, 7].

In an oversampling converter, the same noise power produced as a Nyquist-rate converter is uniformly distributed between $-f_s/2$ and $f_s/2$, where f_s is the sampling frequency. Because f_s is much greater than the signal Nyquist-rate and the overall quantization error energy is constant, only a small fraction of the total noise power falls in the signal band, which is given by [7, 8, 9]

$$P_E = \int_{-f_b}^{f_b} \left(\frac{\Delta^2}{12} \cdot \frac{1}{f_s} \right) df = \frac{\Delta^2}{12} \cdot \frac{2f_b}{f_s} = \frac{\Delta^2}{12} \cdot \frac{1}{OSR} \tag{2.1}$$

where OSR is the oversampling ratio, f_b is the signal bandwidth. $\Delta^2/12$ is actually the quantization noise power of a Nyquist converter where Δ is the quantizer step size.

For an N-bit quantizer with 2^N quantization levels, the maximum signal power equals

$$P_S = \left(\frac{2^N \cdot \Delta}{2\sqrt{2}} \right)^2 = \frac{\Delta^2 \cdot 2^N}{8} \tag{2.2}$$

Thus the maximum signal-to-noise ratio of an oversampling converter is given by

$$SNR_{max} = 10\log\left(\frac{P_S}{P_E}\right) = 6.02N + 1.76 + 10\log(OSR) \quad (2.3)$$

The last term is the *SNR* increment due to the oversampling, while the sum of the first two terms represents the *SNR* resulting from an N-bit quantizer. Increasing the quantizer bit-resolution N and the oversampling ratio *OSR* results in an enhanced *SNR*. However, when taking the advantage of the inherent linearity of a 1-bit quantizer (N = 1), the oversampling alone usually cannot make the *SNR* high enough with a practical sampling rate. For efficiency, noise-shaping needs to be introduced to help achieve a high resolution.

2.2.2 Noise-Shaping

Using the feedback loop configuration illustrated in Figure 2.2, noise-shaping in a ΣΔ modulator increases the baseband signal-to-noise ratio by virtue of attenuating quantization noise at low frequencies [5, 7].

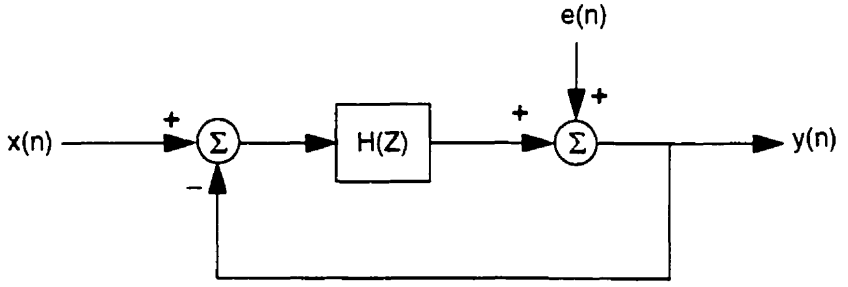

Fig. 2.2: Modulator Linear Model

Treating this modulator linear model under the assumption that *x(n)* and *e(n)* are the two independent inputs, the corresponding output signal transfer function in frequency domain can be described by [10, 11]

$$Y(Z) = F_X(Z) \cdot X(Z) + F_E(Z) \cdot E(Z) \quad (2.4)$$

where $F_X(Z)$ and $F_E(Z)$ denote the signal and the noise transfer functions. With a single loop filter $H(Z)$, they are given by [11]

$$F_X(Z) \equiv \frac{Y(Z)}{X(Z)} = \frac{H(Z)}{1 + H(Z)} \tag{2.5}$$

$$F_E(Z) \equiv \frac{Y(Z)}{E(Z)} = \frac{1}{1 + H(Z)} \tag{2.6}$$

To eliminate noise in the signal base-band, $F_E(Z)$ should be a high-pass transfer function, which implies a low-pass $H(Z)$ because the poles of $H(Z)$ are the zeros of $F_E(Z)$. When $H(Z)$ is chosen to be a typical unity-gain discrete-time integrator as described in Equation (2.7), $F_X(Z)$ turns out to be the Z-transform expression of a pure delay, while $F_E(Z)$ is a first-order high-pass response. The output signal transfer function is given by Equation (2.8) [2, 5, 15].

$$H(Z) = \frac{1}{Z - 1} \tag{2.7}$$

$$Y(Z) = Z^{-1} \cdot X(Z) + (1 - Z^{-1}) \cdot E(Z) \tag{2.8}$$

This is the realization of first-order noise-shaping with the maximum *SNR* given by

$$SNR_{max} = 10\log\left(\frac{P_S}{P_E}\right) = 6.02N + 1.76 - 5.17 + 30\log(OSR) \tag{2.9}$$

Comparing this result with Equation (2.3) reveals that doubling the sample rate with the first noise-shaping will boost the oversampling payoff to 9 dB or 1.5 bits, whereas without noise-shaping, the payoff is only 3 dB.

Figure 2.3 is the structure of a standard second-order noise-shaping configuration [4]. The input-output relationship can be readily derived, and given in Equation (2.10). The signal transfer function remains the same, whereas the noise transfer function is the square

of that of the first-order noise-shaping. As a result, a better performance can be achieved with the *SNR* enhancement by 15 dB or 2.5 bits for every doubling of sampling frequency as illustrated in Equation (2.11).

$$Y(Z) = Z^{-1} \cdot X(Z) + (1 - Z^{-1})^2 \cdot E(Z) \tag{2.10}$$

$$SNR_{max} = 10\log\left(\frac{P_S}{P_E}\right) \approx 6.02N + 1.76 - 12.9 + 50\log(OSR) \tag{2.11}$$

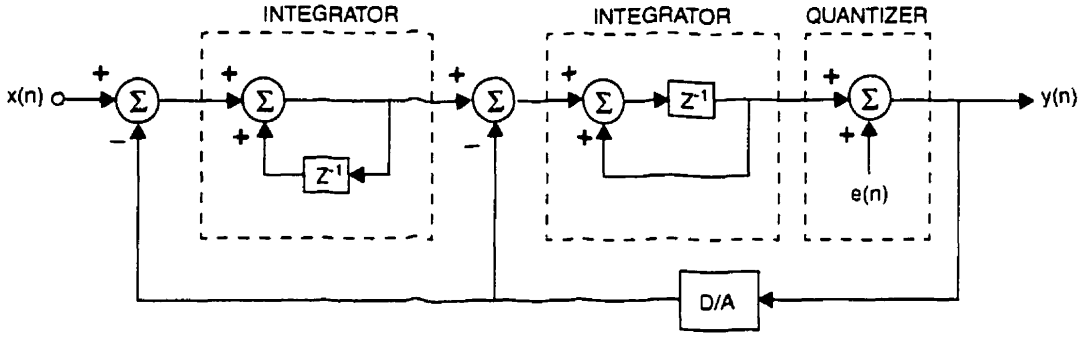

Fig. 2.3: Second-Order Noise-Shaping Structure

The comparison between a first and second order noise-shaping output magnitude spectrum of quantization noise is shown in Figure 2.4 [9, 16].

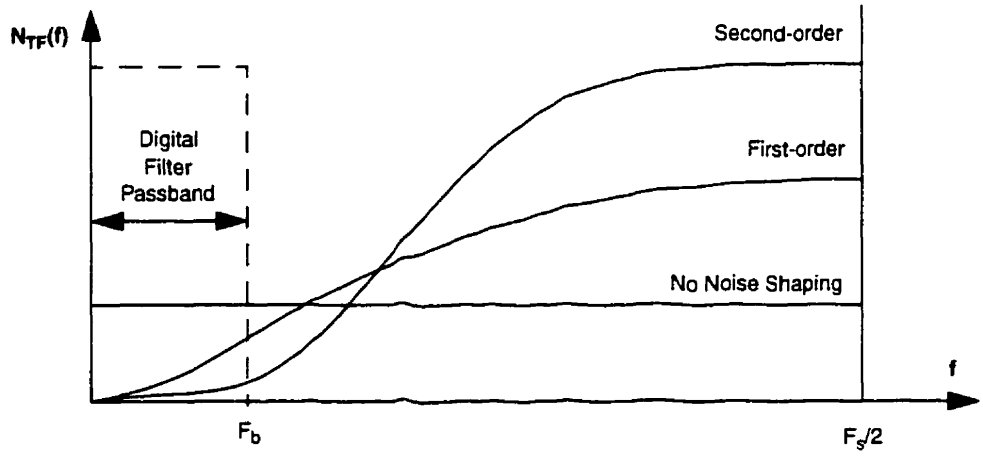

Fig. 2.4: Sigma-Delta Quantization Noise Spectrum

Since the magnitude of the noise transfer function of a second-order modulator is a squared sine wave [7, 9], the in-band quantization noise contributing to the finite resolution of the modulator is further attenuated, while the out-of-band noise is further amplified. The final digital representation thus gets a higher resolution payoff.

Ideally, an nth-order ΣΔ modulator has an output expressed in Equation (2.4) as a linear combination of the input signal $X(Z)$ and the quantization error signal $E(Z)$ with the signal and noise transfer functions $F_X(Z)$ and $F_E(Z)$ given by

$$F_X(Z) = Z^{-n} \tag{2.12}$$

$$F_E(Z) = (1 - Z^{-1})^n \tag{2.13}$$

Basically, higher order noise-shaping leads to lower baseband noise power, thus providing higher signal resolution.

2.3 System-Level Simulation

The objective of this thesis is to design a 15-bit dynamic-range second-order ΣΔ modulator. With a 1-bit quantizer, the oversampling ratio can be estimated to be 80 using Equation (2.9). For audio applications with 8 kHz signal bandwidth, the sampling frequency turns out to be at least 1.28 MHz.

As mentioned before, the linear quantizer model for a ΣΔ modulator has some approximations based on the assumption that actual signal-dependent quantization noise is random white noise. With a second-order noise-shaping, the calculation resulting from Equation (2.9) actually over-estimates the peak *SNR* by about 14 dB according to both Hauser's analysis [11] and Stanley's simulation result [9]. To compensate for this performance reduction, the oversampling ratio needs to be doubled to bring a further 15 dB *SNR* enhancement, so the sampling frequency ends up being 2.56 MHz.

To verify this predicted result, a system-level simulation was performed using Simulink under Matlab* with the set-up configuration shown in Figure 2.5. This block diagram is almost the same as that of Figure 2.3 except for the addition of the three attenuation factors as shown in the modulator diagram in Figure 2.1 to guarantee the modulator system stability. The 1-bit quantizer is realized by a switch, therefore no D/A converter is needed in the feedback loop.

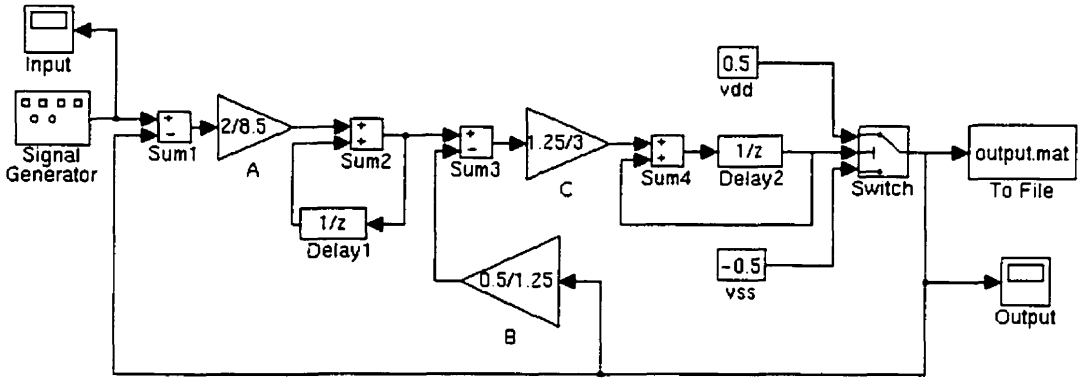

Fig. 2.5: Simulink Set-up Configuration for A 2nd-Order ΣΔ Modulator

To simplify the simulation, vdd and vss were chosen to be + 0.5 V, - 0.5 V respectively when the full scale input voltage was chosen to be 1 V. Figure 2.6 shows the full spectrum of modulator output with a 1 kHz sine wave input signal after the power spectral density function was performed on a sufficient number of samples. A sharp impulse standing for the input signal at the 1 kHz frequency point can be observed obviously, as well as the squared sine noise-shaping effect of the second-order ΣΔ modulator.

Assuming a brickwall filter following the modulator, the signal-to-noise ratio can be calculated from the simulation output data by removing all of the out-of-band frequency power. While modifying the input signal amplitude, the corresponding measured *SNR* can be obtained and the relation between *SNR* versus normalized signal input level can be plotted in Figure 2.7 when a full scale input is normalized to be 0 dB.

* The MathWorks, Inc., Matlab, Version 4.2c, Nov. 23, 1994.

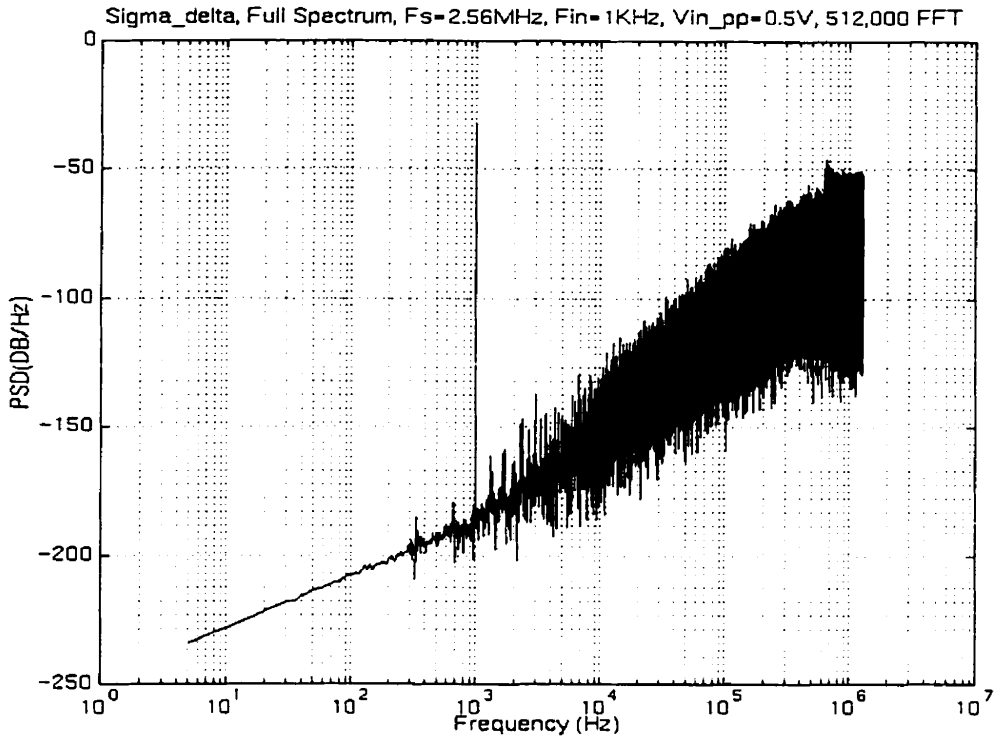

Fig. 2.6: Full Spectrum of Modulator Output

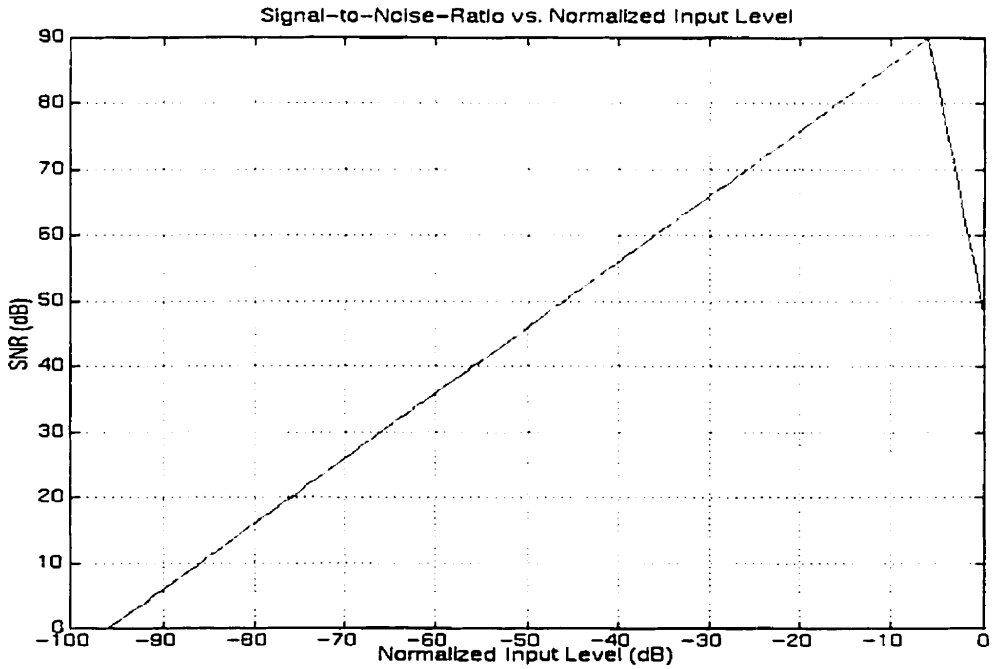

Fig. 2.7: Plot of *SNR* versus Normalized Signal Input level

According to the simulation result, with ideal analog components, a 15-bit dynamic range with 8 kHz bandwidth can be realized by using 1-bit quantizer with a second-order noise-shaping under the sampling frequency 2.56 MHz. The oversampling ratio is 160.

2.4 Modulator Design Considerations

Figure 2.8 shows the practical modulator architecture chosen for the thesis. It differs from the traditional "delay-free" configuration illustrated previously in Figure 2.3, but actually offers important superior practical merits.

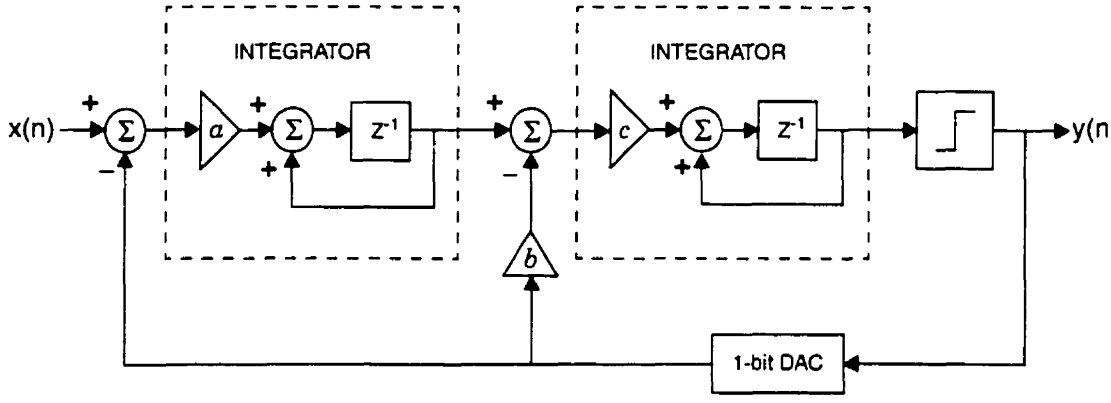

Fig. 2.8: Practical Second-Order Sigma-Delta Modulator

By replacing the first non-delaying integrator with a delaying integrator, the integrators' output probability densities within a full-scale quantizer range become much higher than those in Figure 2.3 [1]. This smaller distribution of the signals on the internal nodes makes this configuration a better choice, especially in low-voltage design where the swing is very limited [14]. In addition, two forward path delays amounting to pipelining between two integrators practically simplify the implementation of the modulator with straightforward sampled-data analog circuits, since each integrating amplifier has one clock cycle to settle. Furthermore, the gain factor a chosen to be less than one half, attenuates the output of the first integrator with the same ratio to potentially improve the dynamic range and linearity of the converter with respect to amplifier saturation [13, 14].

With no additional components and further power dissipation, this modulator topology offers identical noise-shaping with that of Figure 2.3, except for the introduction of an extra delay in the signal transfer function which becomes Z^{-2} instead of Z^{-1} [11 - 13]. The input-output relationship for this architecture is given by Equation (2.14) which is in conformity with the definition of a nth-order ΣΔ modulator described in Equation (2.12) and (2.13).

$$Y(Z) = Z^{-2} \cdot X(Z) + (1 - Z^{-1})^2 \cdot E(Z) \tag{2.14}$$

2.4.1 Stability

In a theoretical modulator shown in Figure 2.8, a proper choice of the gain factors allows not only the design of stable loops, but also the optimization of the loop response for maximum effective resolution.

The gain factor a in the first integrator influences the noise-shaping function and thus the ΣΔ modulator performance. A larger a value means higher gain in the forward path of the modulator and consequently greater attenuation of the quantization noise [1, 3]. This coefficient can vary as much as 20 percent from its nominal value with only a minor impact on the in-band quantization noise, confirming the general insensitivity of the ΣΔ modulator architecture. However, the value of the gain a cannot be larger than 0.6, otherwise the integrator's output amplitude will be increased rapidly and the system will become unstable [1, 3].

In a second-order ΣΔ modulator, the stability is also determined by the ratio a/b. Actual requirements on the precision of the coefficients to obtain an optimized quantization noise response exceeds the requirements for a stable system [2, 3]. The requirement of a stable loop is $a < 0.75b$, whereas the maximum *SNR* happens around the point where $a = 0.5b$ [3, 14]. Generally, the loop coefficients should increase from the first to the last integrator to reduce the internal error accumulations.

In theory, since the second integrator is followed immediately by a two-level quantizer, gain factor c can be adjusted arbitrarily without impairing the performance of the modulator [1]. In practice, c is chosen to make sure that the signals are not clipped in a real implementation [14].

In switched-capacitor integrators, these coefficients are very conveniently achieved by adjusting the ratio of capacitors to accommodate easier implementation and better *SNR* performance without jeopardizing the modulator stability.

2.4.2 Noise Sources

The performance of a ΣΔ modulator is not only determined by the in-band quantization noise as theoretically analyzed in section 2.3, but is also influenced by the circuit noise associated with solid-state devices in physical implementation. Since the circuit noise generated in the internal nodes of a ΣΔ modulator loop is strongly suppressed by the high loop gain, the one injected into the input summing node plays a dominant role. As a result, the circuit noise of the converter is almost completely determined by the noise of the first integrator. The main circuit noise sources of a silicon implementation are thermal noise and flicker noise [14, 17, 18].

I. Thermal Noise

Thermal noise is due to the thermal excitation of charge carriers in a conductor. It has a white spectral density and is proportional to absolute temperature. In a sampled data ΣΔ modulator, the thermal noise is generated by the on-resistance of the switches in the sampling and integrating process. When a fully differential switched-capacitor integrator is used, the main thermal noise power is given by [18]

$$P_T = \frac{4KT}{C_S \cdot OSR} \tag{2.15}$$

where K is Boltzmann's constant, T is the absolute temperature, and C_S is the sampling capacitance. Obviously, thermal noise can be diminished by choosing a larger sampling capacitor or a larger *OSR*.

II. Flicker Noise

Flicker noise is due to the random trapping and de-trapping of majority carriers in the channel of MOS devices. It is commonly referred to as $1/f$ noise because the fluctuations in the channel charge carrier density have a relatively large time constant [7, 8]. The normalized power of a single active MOSFET is given by

$$P_F = \frac{K_F}{WLC_{OX}f} \tag{2.16}$$

where K_F is a constant which depends on process characteristics, W and L are the transistor's width and length respectively, and C_{OX} represents the gate capacitance per unit area. Typically NMOS devices demonstrate a higher flicker noise than PMOS counterparts since their majority carriers (electrons) are likely to be trapped [7, 8]. As a result, flicker noise can be diminished mainly by using PMOS as input devices with large device size. Chopper stabilization and correlated double sampling techniques can also be employed to provide a first-order flicker noise cancellation [8, 14, 18].

III. Noise Contributions

Figure 2.9 represents schematically the different noise levels contributed in a ΣΔ modulator, where f_B indicates the signal base-band. The final *SNR* of a ΣΔ modulator is determined by the ratio of signal power to both the quantization noise and the circuit noise, which includes thermal and flicker noise. In practice, quantization noise and thermal noise are usually the main considerations, whereas flicker noise can be made low enough with a careful circuit design so as not to degrade the modulator performance significantly [17].

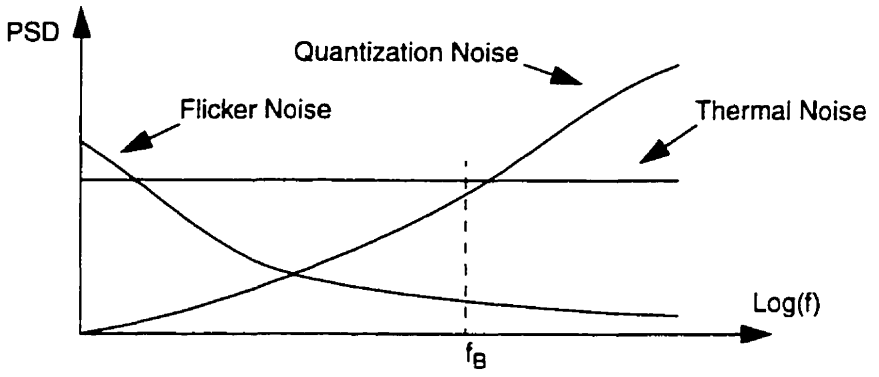

Fig. 2.9: Noise Power Spectral Densities

2.4.3 Power Dissipation

As mentioned previously, a ΣΔ modulator's noise level can be diminished by choosing a higher *OSR*, a higher modulator order, or a larger sampling capacitor. But each of these requires an extra power allocation.

A higher *OSR* requires all the integrators to settle faster, thus slew rates and gain bandwidth products must be increased. This implies an increased current thus an increased power consumption. To a first-order approximation, doubling the *OSR* causes double the power consumption in a ΣΔ modulator [14].

A higher modulator order brings extra circuits and power dissipation for a ΣΔ modulator because each additional modulator order requires one extra integrator in switched-capacitor circuits.

A larger sampling capacitor results in an increased integrator loading capacitance which implies the increasing current with the same order [14]. Therefore, the smallest capacitor sizes for which the required converter resolution and bandwidth can be maintained should be used. The first integrator dominates the power dissipation because it is limited by kT/C noise and must settle to the accuracy of the overall modulator independent

of *OSR*. Subsequent integrators may employ smaller capacitors and settle less accurately, which reduces their power dissipations [19].

Operating at reduced supply voltages is not advantageous from a power dissipation perspective for analog circuits whose dynamic range is kT/C limited because the capacitor values need to be increased as the inverse square of the power supply voltage to preserve the same dynamic range. This not only cancels any advantage accrued in dynamic power dominated by CV^2, but also again implies increased current. But balanced against this fundamental consideration is the fact that, since analog circuits reside only as a small cell, in many current mixed-signal systems, large digital portions dominate the overall power dissipation, which benefits from the combination of scaled technology and reduced supply voltages.

2.4.4 Switches

The behavior of a switch is of great importance in switched-capacitor circuits because it may limit both the input signal range and the obtainable operating frequency.

The input signal must be operating in such a range that the driving signal can turn on the switch at any input signal level. Although in one MOS transistor switch, this range is limited by the gate driving voltage and the MOS threshold voltage, a CMOS transmission gate allows the passage of a rail-to-rail input signal, which is thereby an exact choice in switched-capacitor circuits. The circuit operating frequency is influenced by the time constant defined by the switch on-resistance together with the sampling capacitor [39]. The on-resistance should be as small as possible to meet the speed requirement.

The gate driving voltage plays an important role in the switch performance. Although a low-supply voltage results in a great power saving for digital circuits, it creates a switch driving problem for analog switched-capacitor circuits. For a CMOS switch, the gate driving voltage must be larger than the sum of NMOS threshold voltage V_N and PMOS

threshold voltage V_P. Further consideration of the transistor's body effect requires the gate driving voltage to be even higher. For a low supply voltage condition where $V_{DD} < V_N + V_P$, a bootstrapping circuit using charge pumps must be introduced which can increase the driving voltage approximately up to $2V_{DD}$ [18, 20].

A large on-resistance due to low gate driving voltage can be reduced by increasing the transistors' width over length ratio. But a larger transistor size induces a larger charge injection [40]. In CMOS transmission gates, the charge injection can be partially cancelled because of the opposite charges produced by both NMOS and PMOS transistors. For the switches used between integrators and comparators in a modulator, the charge injection can be further significantly reduced by the fully differential configuration and the proper turning on/off sequences [1, 7, 36].

Linearity is another important factor in the design of the switches. The switches should operate with a relatively constant on-resistance, independent of the input voltage. In a CMOS transmission gate, PMOS should be larger than NMOS by a factor around their mobility ratio. The final choice of switch size is based on the trade-off between the desire to reduce the series RC time constant, the switch linearity, and the requirement to keep parasitic and charge injection effects negligible [40].

2.4.5 Dynamic Range, SNR and SNDR

When evaluating the performance of a ΣΔ modulator, three main related specifications are Dynamic range, *SNR* and *SNDR*. The dynamic range of a modulator is defined as the ratio of the power in a full-scale input to the power of a sinusoidal input for which the signal-to-noise ratio (*SNR*) is one. It is the ratio in power between the maximum input signal level that the modulator can handle and the minimum detectable input signal. *SNR* is the ratio of the output signal power to the noise power, which includes all noise sources in the modulator. *SNDR* is the ratio of the output signal power to the sum of the noise and

harmonic distortion powers. For small signal levels, distortion is not important, implying that the *SNR* and *SNDR* are approximately equal. As the signal level increases, the precision of the converter is limited by harmonic distortion rather than quantization noise. Distortion degrades the modulator performance, so the *SNDR* will be less than *SNR* [1].

In a modulator with performance limited by circuit noise, higher supply voltages improve the dynamic range due to the increased signal power and a constant thermal noise floor. For a low-supply voltage design, the input-signal amplitude must be maximized to maximize the dynamic range. In practice, the maximum input amplitude is typically limited to a fraction of the feed back reference levels to ensure the stability of a second-order ΣΔ modulator [18].

As mentioned before, coefficients *a*, *b*, and *c*, in Figure 2.8, not only determine the modulator stability, but also influence the modulator dynamic range. Peluso [21] provided a detailed analysis on the topology coefficients that yield the best performance in terms of dynamic range. Generally, within the boundaries of stability requirements, a constant product of integrator gains yields approximately equal performance, while the maximum dynamic range is found close to the stability border. In a second-order ΣΔ modulator, as mentioned in section 2.4.3, the coefficients' requirements for an optimized dynamic range is $a = 0.5b$, exceeding those for stability.

2.4.6 Input Full-Scale Range

The choice of a full-scale analog input range for the converter involves trade-offs among a number of important design constraints. A large signal range results in a large dynamic range [22], but also an increased harmonic distortion due to the integrator nonlinearity [1]. Increasing the signal range may call for the opamp with slew limiting [23]. To avoid significant performance degradation, the full-scale analog input signal range is usually smaller than 2 / 3 signal range at the outputs of both integrators [1].

2.5 Integrator Design Considerations

In Figure 2.8, a second-order ΣΔ modulator consists of two integrators, which can be realized by non-inverting, delaying, discrete-time, switched-capacitor integrators with the principle architecture shown in Figure 2.10 [7, 37].

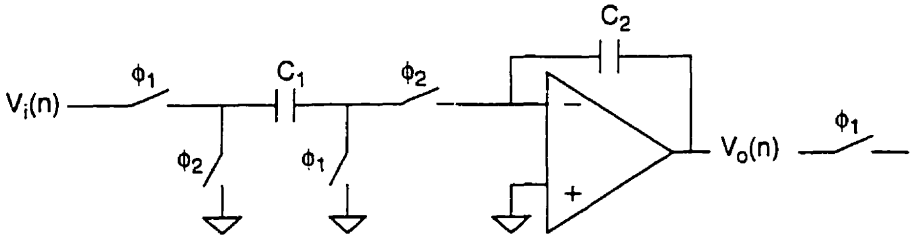

Fig. 2.10: Switched-Capacitor Integrator Architecture

This integrator has an advantage of being insensitive to parasitic capacitances with the transfer function given by

$$H(Z) = \frac{V_O(Z)}{V_I(Z)} = \frac{C_1}{C_2} \cdot \frac{Z^{-1}}{1 - Z^{-1}} \tag{2.17}$$

In a ΣΔ modulator, the integrators' performance is specified in terms of non-idealities that limit the overall modulator dynamic range and operation speed. Parameters such as finite DC gain, linear settling, and slew rate can raise the quantization noise floor and introduce distortion. The available swing at the output sets the modulator peak input signal handling capability. Thermal noise introduced by the sampling capacitors as well as by the amplifiers adds directly to the quantization noise to set the minimum detectable signal. Switched-capacitor integrators are the key circuit building blocks in a ΣΔ modulator [24].

2.5.1 Amplifier Topology

The choice of amplifier topology plays a critical role in a low-voltage, low-power integrator design. The desired main characteristics include maximum output swing, minimum number of current legs from a power-dissipation perspective, high gain for the linearity, enough bandwidth with high slew-rate, and a minimum number of devices that contribute significant thermal noise [19].

The two basic topologies are the folded cascode and the two-stage class A amplifier. The folded cascode topology has a higher gain and higher non-dominant pole, thus providing higher frequency performance [35]. But it has lower output swing, which is especially critical to a low-voltage design. The two-stage class A amplifier with a larger swing and lower non-dominant pole meets our low-frequency modulator application, but its gain is lower. So the two main topologies are combined together in this thesis to realize a two-stage, pole-split compensation amplifier with high gain, large output swing and relatively low frequency response [18, 26, 29].

A fully differential configuration is adopted for the integrator implementation not only because of its improved power supply rejection ratio (*PSRR*) [41, 51], and reduced clock feed through and switch charge injection errors [7, 38], but also because of its net gain of 3 dB in the signal-to-white noise ratio with respect to a single-ended version, resulting from the duplicated array of input capacitors [17, 27].

2.5.2 Integrator DC Gain

The integrator described by equation (2.17) has an infinite opamp DC gain which, in practice, is limited by circuit constraints. A finite opamp DC gain causes the inverting opamp terminals to reflect the output voltage rather than behave as a virtual ground [2, 28]. Consequently, not all of the charge on the sampling capacitors will be transferred to the integrating capacitors, resulting in a "leaky integration". This effect is a linear process and

can be incorporated into the linear switched-capacitor integrator model by adding leakage and integration gain coefficients. The realistic transfer function of the integrator is given by [1, 9]

$$H(Z) = \frac{V_O(Z)}{V_I(Z)} = \frac{C_1}{C_2} \cdot \frac{Z^{-1}}{1 - P_o Z^{-1}} \tag{2.18}$$

where P_o is a fraction of the previous output added to each new input sample. Obviously the finite DC gain introduces simultaneously a gain and a pole error in the integrator transfer function. The gain error limits the perfect cancellation of the quantization noise, while the pole error creates noise leakage at low frequency [17]. The limited gain at low frequency reduces the attenuation of the quantization noise in the baseband, and results in an increase of the in-band noise by a factor of β, given by [1, 9]

$$\beta = \frac{5}{\pi^4} \cdot \left(\frac{OSR}{A_{DC}}\right)^4 + \frac{10}{3\pi^2}\left(\frac{OSR}{A_{DC}}\right)^2 \tag{2.19}$$

where A_{DC} is the opamp DC gain. When A_{DC} is comparable to *OSR*, the *SNR* penalty is on the order of 1 dB [25]. If the opamp DC gain drops below *OSR*, there will be a significant *SNR* degradation with the rapidly increased quantization noise [19, 26, 30, 31]. In practice, the DC gain must be larger than the *OSR* order to adequately suppress harmonic distortion. When the DC gain to *OSR* ratio is larger than 10, the related baseband error is gain-independent and can be negligible [25].

2.5.3 Integrator Linear Settling and Slew Rate

During every clock cycle, a switched-capacitor integrator steps to a new output level with an exponential response in nature. However, if the step size is large enough, slewing occurs due to the maximum current that an opamp can drive, and the integrator settles with a combination of slew and exponential characteristics [2].

Linear settling and slew rate specify the small-signal and large-signal speed performance of an integrator respectively. In a ΣΔ modulator, a linear settling error results in an integrator gain error, and a limited slew rate results in harmonic distortion, which directly degrades the large signal performance of a modulator [24, 30, 32].

Although an integrator needs a sufficient bandwidth for the signal to settle within a half clock period, sigma-delta modulators can achieve high resolution performance even if the integrators do not settle to the full resolution of the converter, as long as the settling process is linear and the settling is not slew-rate limited [1, 18]. In a switched-capacitor integrator, the settling time constant is a function of switches' on-resistance and the amplifier's load which is equal to the integration capacitor in series with the parallel combination of the sampling capacitor and the input transistors' capacitance. Thus, the input transistor size that minimizes the settling time constant depends on the sampling capacitor size [18].

The slew rate is also a function of the amplifier's load capacitance. Sufficient slew rate can make the degradation of *SNR* negligible [2]. For a second-order ΣΔ modulator, Boser's simulation [1] shows that the minimum amplifier's slew-rate must be $3\Delta/T_S$, where Δ is the input full scale, and T_S is the sampling clock period.

Increasing slew rate and reducing settling time can be realized by using smaller capacitances. However, the reduction in capacitor size is limited not only by kT/C noise, but also practically by matching considerations as well as the combination of parasitic capacitance which becomes more severe particularly at the amplifier's input.

2.5.4 Integrator Unity Gain Frequency and Phase Margin

In a typical sampled-data analog integrator, the unity gain frequency of the opamp must be at least an order of magnitude greater than the oversampling rate [1]. However, as indicated in section 2.5.3, a lower unity gain frequency with a correspondingly inaccurate settling will not impair the ΣΔ modulator performance if the settling process is linear. For an

ideal integrator with a single dominant pole exponential impulse response, the response time-constant τ can be as large as the sampling period T_S [1]. A value of τ that is larger than T_S will make the $\Sigma\Delta$ modulator unstable.

In practice, however, because the settling process usually includes a signal-dependent slewing component, and is influenced by non-dominant poles and the dependence of the pole locations on the amplifier operating point, as well as finite switch resistances in the switched-capacitor network [25], the integrator cannot operate with an exponential impulse response. Also considering non-overlapping clocks with duty cycle slightly less than a half clock period, the unity gain frequency must be at least twice the sampling rate [1]. As a general rule of thumb, the unity gain frequency should be around 5 times the sampling clock frequency [7, 20], with a phase margin greater than 70 degrees to provide a smooth settling characteristic [1, 7, 33].

2.5.5 Integrator Output Swing and Offset

An operational amplifier's output swing defines the maximum signal handling capability and is directly related to the modulator input level. Maximizing the output swing will increase the maximum dynamic range, at the same time, minimizing the required sampling capacitance and power dissipation as described in section 2.4.3.

The output swing, ultimately limited by the power supply voltage, is even more critical in a low-voltage design. In practice, the output swing is lower than the supply voltage because the output devices must operate in active region. To maximize the output swing, a common source output configuration must be used and a switched-capacitor common-mode feedback circuit must be applied when using a fully-differential amplifier configuration [7].

In a second-order $\Sigma\Delta$ modulator, offset is only a minor concern as long as the quantization is uniform [1]. The offset at the input to the first integrator is the only significant contributor because offsets in the second integrator and the comparator are

suppressed by the large low-frequency gain of the integrators. In practice, to avoid large reduction in the effective signal range, offsets should not be excessive.

2.6 Comparator-Latch Design Considerations

In the forward path of a ΣΔ modulator, the 1-bit quantizer can be realized by a track-and-latch comparator, which consists of a regenerative latch and a preamplify stage which helps to increase resolution and reduce clock kickback effects [29, 37]. Kickback denotes the charge transfer either into or out off the comparator inputs when the track-and-latch stage goes from the track mode to the latch mode. The charge transfer is caused by the charge needed to turn on the transistors in the positive-feedback circuitry and by the charge that must be removed to turn off the transistors in the tracking circuitry. Without a preamplifier, this kickback will affect the driving circuitry and cause large glitches, especially when the two inputs are not perfectly matched.

The main parameters of the comparator-latch design to consider are speed, input offset, input-referred noise, and hysteresis.

The comparison speed must be high enough to meet the desired sampling rate. Minimum channel length must be used for all transistors in a comparator-latch. The gain of the preamplify stage should not be too large to limit the comparison speed [7].

The offset and input-referred noise at the comparator input can be suppressed by the feedback loop of the ΣΔ modulator [33, 34]. Using PMOS transistors with large size in preamplify stage also results in smaller flicker noise contribution [36].

The comparator hysteresis is very important for the modulator operation [17]. Defined as the minimum overdrive required to change the output, it can be modeled as an additive white noise at the input of the comparator [1, 28, 33], and can be shaped out-of-band in the same way as the quantization noise by the feedback loop [28, 34]. When the hysteresis is

less than 10 percent of the full-scale converter input, the in-band noise power is signal-independent and virtually unchanged, and has a negligible impact on the modulator performance according to Boser's simulation [1].

2.7 Clock Signals

Switched-capacitor integrators require two-phase non-overlapping clocks with delayed versions to minimize signal-dependent charge injection errors [7, 24]. The comparator-latch also needs these clock signals to separate the reset and track phases. Appropriate non-overlapping periods must be provided between the clocks to allow sufficient amplification of the input signal of the comparator [41]. As shown in Figure 2.11. ϕ_1 and ϕ_2 are the waveforms of the two-phase clock, ϕ_{1d} and ϕ_{2d} are the delayed versions.

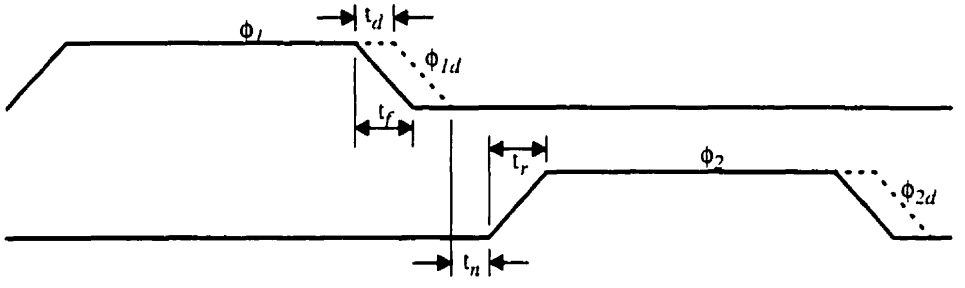

Fig. 2.11: Timing Waveforms of Two-Phase Non-overlapping Clocks

The rising edges of the delayed clocks should be lined up with the rising edges of the non-delayed versions to increase the amount of available settling time for the integrators. The available settling time T_{AS} is given by

$$T_{AS} = \frac{T_S}{2} - t_n - t_r - t_f \tag{2.20}$$

where T_S is the sampling clock period, t_n is the non-overlapping time, t_r is the rise time, and t_f is the fall time, as shown in Figure 2.11.

2.8 Summary

This chapter provides an overview of the theory and design principles of a second-order sigma-delta modulator. The theory of oversampling and noise-shaping were introduced, and demonstrated by the system-level simulation. The main considerations and trade-offs of a modulator design were discussed in detail, as well as the required specifications of the integrator that primarily determine the modulator's performance. The design considerations of the comparator-latch and the driving clock signals were also discussed. The transistor-level design of a modulator implementation, which will be provided in Chapter 3, is based on the criteria described in this chapter.

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CHAPTER 3

Modulator Design and Implementation

The second-order ΣΔ modulator, illustrated in Figure 3.1, was designed and implemented using a 3.3 V, 0.35μm CMOS technology. The building blocks include the bias circuit, the operational amplifier, the comparator-latch, and the clock generator. These building blocks are discussed in the following paragraphs.

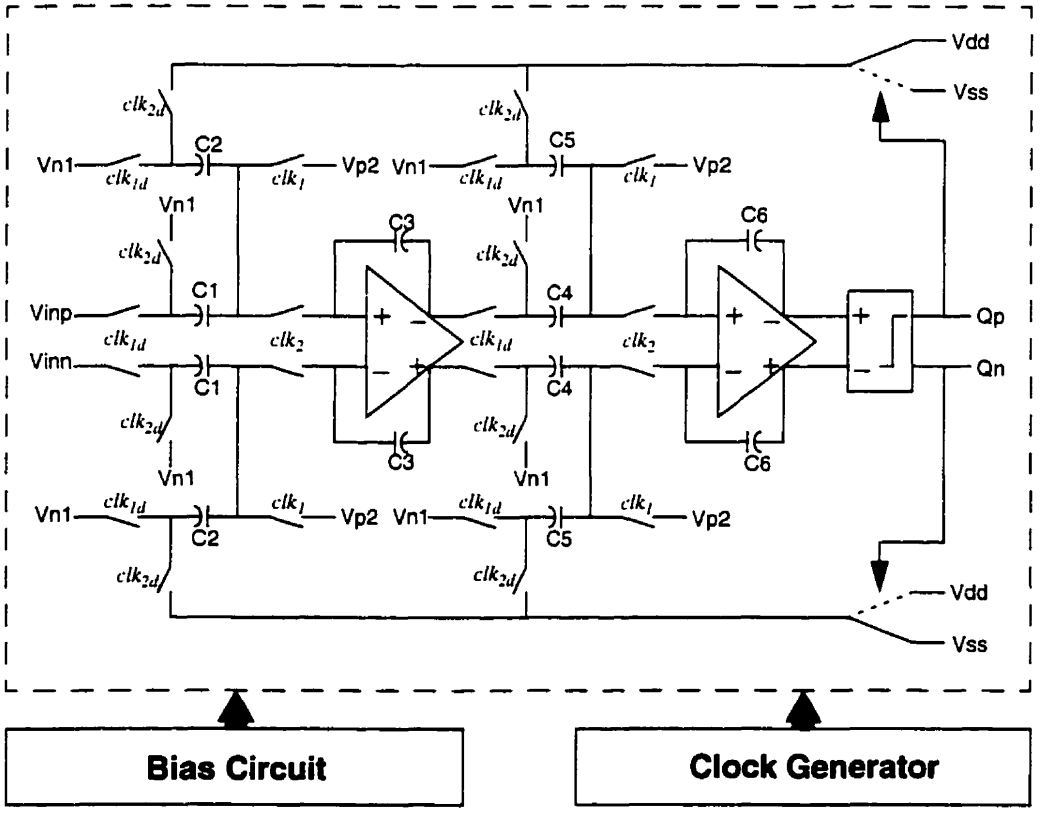

Fig. 3.1: Block Diagram of the Second-Order Sigma-Delta Modulator

3.1 Bias Circuit

The bias circuit is critical for the modulator. It provides and determines the basic operating points for both the operational amplifier and the comparator, and the reference voltages for the modulator.

3.1.1 Architecture

The architecture of the bias circuit is shown in Figure 3.2. It is essentially a modified constant-transconductance bias stage that is suitable for low-voltage applications with a collection of high-swing cascode current mirrors connected in several feedback loops.

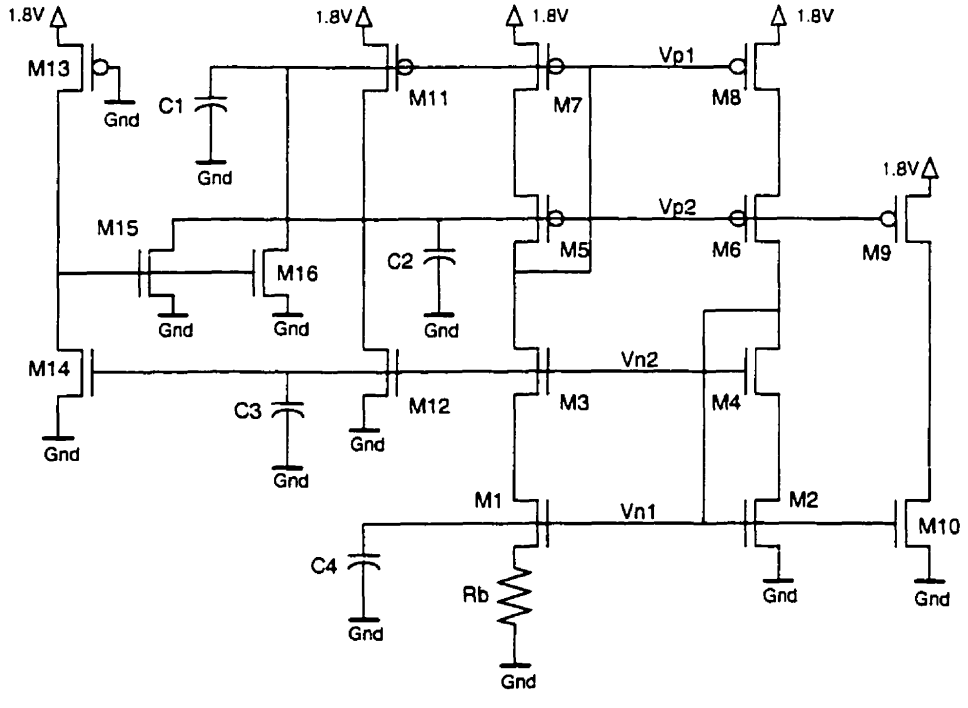

Fig. 3.2: Bias Circuit Architecture

Four bias voltages are provided by the bias circuit. Vp1 and Vn1 are for the single-stacked devices of the opamp, while Vn2 is for the opamp's "wide-swing" cascode NMOS

devices. Vn1 is chosen to be the mid-rail voltage (0.9 V) because it is necessary for both the common-mode feedback circuit and the realization of the final sigma-delta modulator. Vp2 (0.4 V) serves as the common-mode input reference voltage for the opamp.

Transistors M13 to M16 serve as a start-up circuit. Four capacitors C1 to C4 are attached at every bias voltage output to make it stable. Rb is an off-chip bias resistor used to set the transconductance of M2. Component values are listed in Table 3.1. With all the transistors working in the active region, all device transconductances track, to a first degree, over power supply, process, and temperature variations [1, 2].

Table 3.1: Bias Circuit Component Values

Transistor	W/L (μm/μm)	Transistor	W/L (μm/μm)
M1	6/0.7	M10	3/0.7
M2	1.5/0.7	M11	36/1.4
M3, M4	3/0.7	M12	0.7/0.7
M5 to M8	18/1.4	M13	2/18
M9	3.8/1.4	M14 to M16	3/0.7

C1 to C4	1 pF	Rb	7.8 kΩ

3.1.2 Layout

Figure 3.3 shows the layout of the bias circuit. Its area is 128x64 μm^2. The four capacitors occupy 2/3 of the layout area. The basic bias circuit is on the upper left hand side of the layout, while the switch circuit used as an interface for off-chip bias voltages occupies the lower left hand side of the layout.

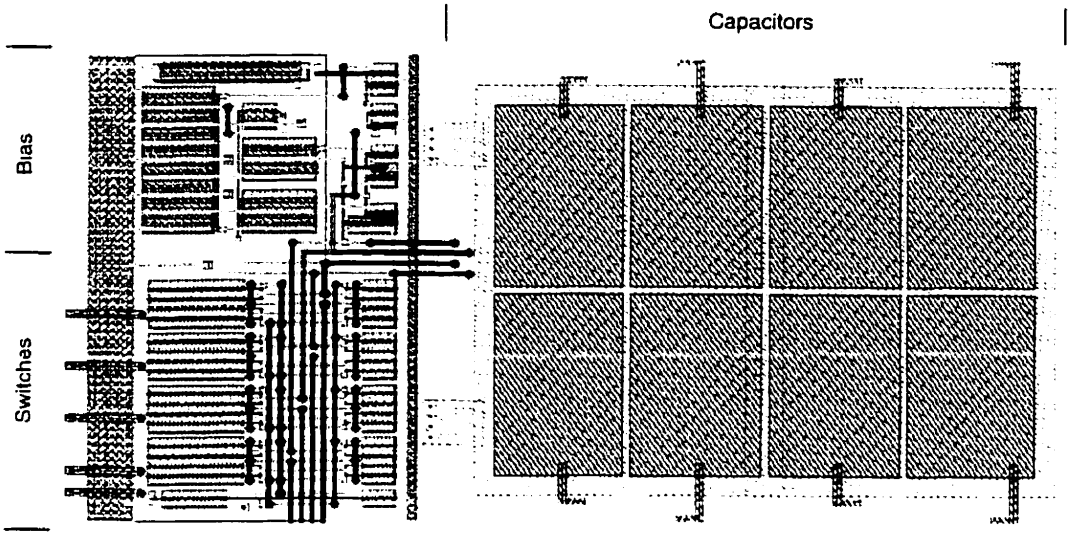

Fig. 3.3: Layout of Bias Circuit

3.1.3 Simulation Results

Table 3.2 lists the four output voltages and the power dissipation from the post-layout simulation of the bias circuit.

Table 3.2: Post-layout Simulation Results of Bias Circuit

Parameter	Value
Vn1	0.899 V
Vn2	1.239 V
Vp1	0.865 V
Vp2	0.398 V
Power Dissipation	173.7 μW

3.2 Operational Amplifier

In a ΣΔ modulator design, the operational amplifier is the most important component that determines the accuracy of the discrete-time integrator, thus determining the performance of the final ΣΔ modulator.

3.2.1 Architecture

A fully differential configuration was adopted for the operational amplifier, which consists of a differential stage and a common-mode feedback stage.

1. Differential Stage

The differential stage was realized by a folded-cascode input stage followed by a common-source output stage, as shown in Figure 3.4.

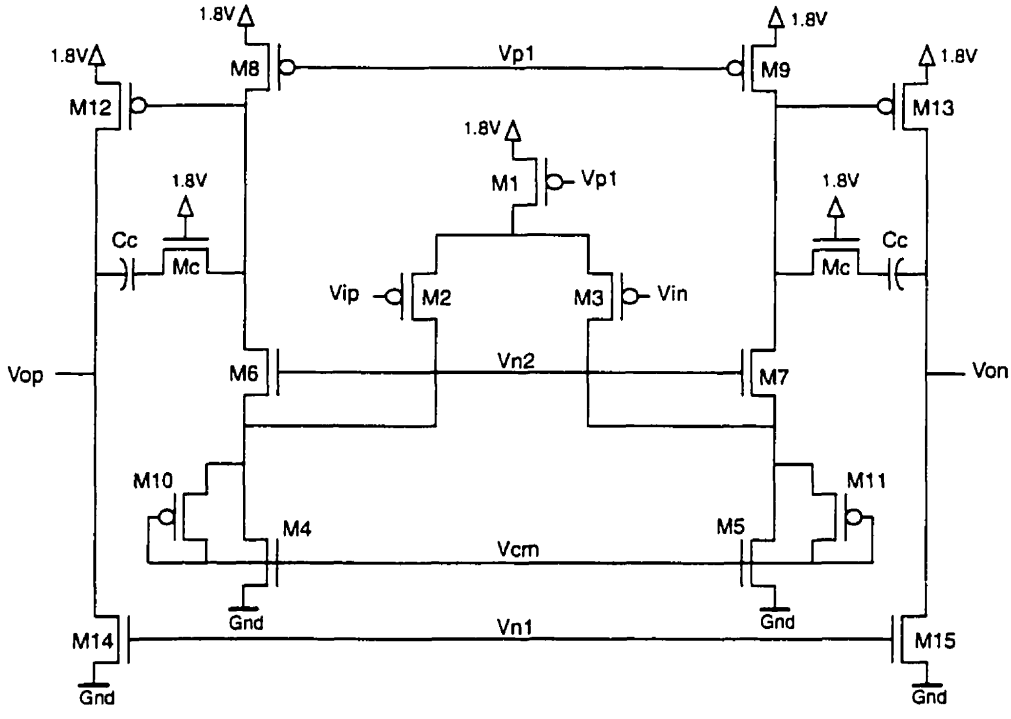

Fig. 3.4: Differential Stage of Operational Amplifier

Vip and Vin are the inputs signals. Vop and Von are the differential outputs. M2 and M3 are the PMOS input transistors. M1, M8, M9, M14, and M15 are the bias transistors. M10 and M11 are used to improve the slew-rate limiting. Transistors Mc and capacitors Cc are used to realize lead compensation for both the differential and the common-mode feedback paths. M4 and M5 are the current sources controlled by the common-mode feedback voltage Vcm generated by the common-mode feedback stage. Table 3.3 lists the device parameters in the differential stage. The value of Cc is 2.3 pF.

Table 3.3: Differential Stage Component Values

Transistor	W/L (μm/μm)	Transistor	W/L (μm/μm)
M1	72/1.4	M8, M9	18/1.4
M2, M3	90/0.7	M10, M11	9/0.7
M4, M5, M14, M15	4.5/0.7	M12, M13	54/1.4
M6, M7	3/0.7	Mc	12/0.7

Because of the lack of a PMOS cascode stage, the channel lengths of M8 and M9 were chosen to be large enough to meet the gain requirement. Due to the fact that the input PMOS threshold voltage is around 0.8 V (including body effects), and that a single 1.8 V power supply is used, the input common-mode voltage of the opamp was chosen to be 0.4 V to ensure a large input signal swing.

2. Common-Mode Feedback Stage

The common-mode feedback stage includes a switched-capacitor network followed by an inverting amplifier, as shown in Figure 3.5. The switched-capacitor network is a power-saving method that ensures a large output swing which is very important in a low-voltage design [2].

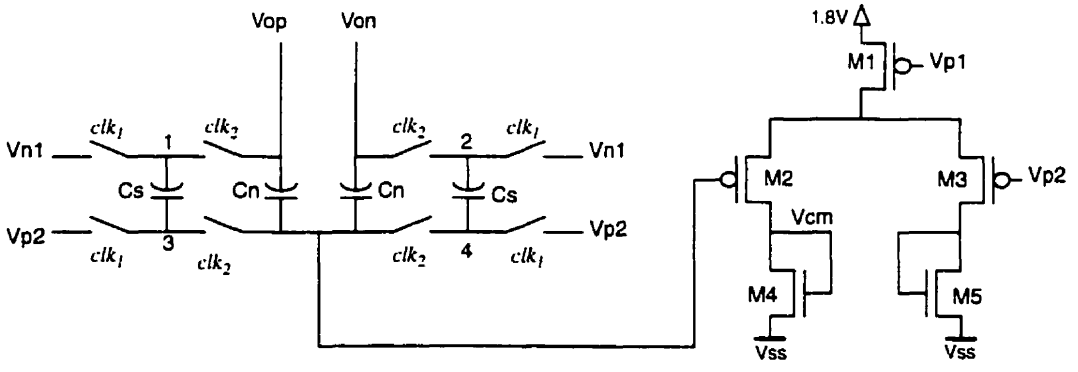

Fig. 3.5: Common-mode Feedback Stage

Vcm is the common-mode feedback voltage generated by this common-mode feedback stage. It is applied to the gates of transistors M4 and M5 in Figure 3.4 to ensure a large common-mode loop gain. The differential outputs Vop and Von are averaged through the non-switched capacitors labelled Cn, and the DC levels are maintained through the switched capacitors labelled Cs [1, 2, 8].

In Figure 3.5, the switches connected to nodes 1 and 2 are realized by CMOS transmission gates to accommodate a wider output swing. The switches connected to nodes 3 and 4 can only be implemented using an NMOS pass transistor because of the low reference voltages (Vp2 = 0.4V). The on-resistance of each switch must be as small as possible. To realize a high speed performance, the transistor channel length of all the switches is chosen to be minimum.

The capacitors Cn and Cs affect the slew rate and the phase margin of the opamp. Normally Cs is chosen to be smaller than Cn [1]. Table 3.4 lists the component parameters in the common-mode feedback stage.

Table 3.4: Common-mode Feedback Stage Component Values

Transistor	W/L (μm/μm)	Capacitor	Value
M1	36/1.4	Cn	500 fF
M2, M3	30/0.7	Cs	200 fF
M4, M5	1.5/0.7		

3.2.2 Layout

The layout of the operational amplifier is shown in Figure 3.6. Its area is 420x130 μm^2. Most of the area is occupied by the capacitors. Three more binary-weighted capacitors ranging from 0.5 pF to 2 pF were generated and connected parallel to the compensation capacitors Cc by switches. So the compensation capacitance can be changed to compensate for the possible effects of processing variations when the chip is being tested.

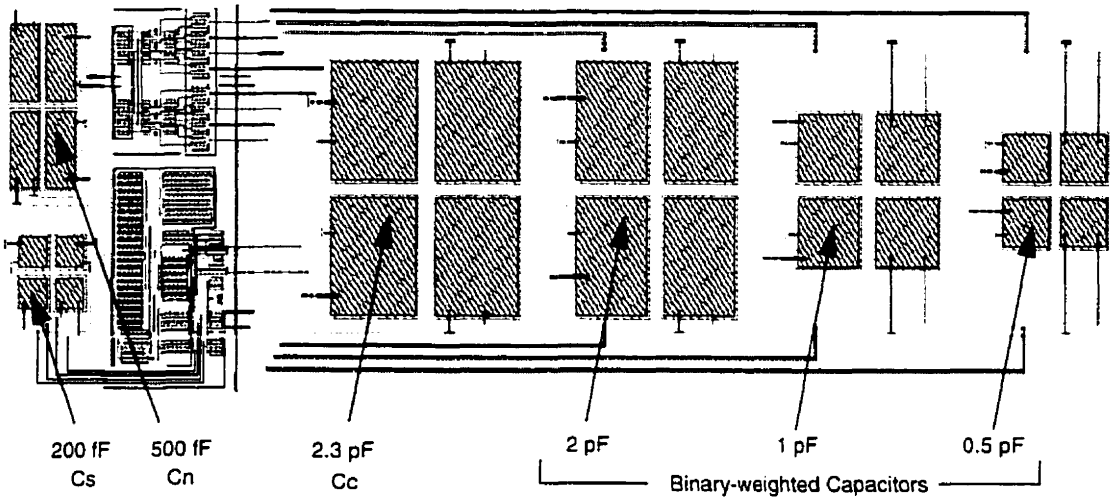

Fig. 3.6: Layout of Operational Amplifier

3.2.3 Simulation Results

Figure 3.7 shows the post-layout simulation of the operational amplifier frequency response. The solid lines indicate the AC analysis of the differential path, while the dashed lines show that of the common-mode feedback path. The performance characteristics of the operational amplifier is summarized in Table 3.5. According to the criteria described previously in Chapter 2, all necessary performance requirements of the operational amplifier are met for a sampling rate of 2.56 MHz.

Table 3.5: Operational Amplifier Performance Characteristics

Parameter	Requirement	Differential Stage	Common-mode Feedback Stage
DC Gain	> 64 dB	88.5 dB	83.7 dB
Phase Margin	> 70 Degree	73 Degree	82 Degree
Unity-gain Frequency	> 12.8 MHz	25 MHz	16 MHz
Slew Rate	> 21.6 V/μs	31.7 V/μs	
Settling Time	< 173 ns	150 ns	
Power Dissipation	-	400 μW	

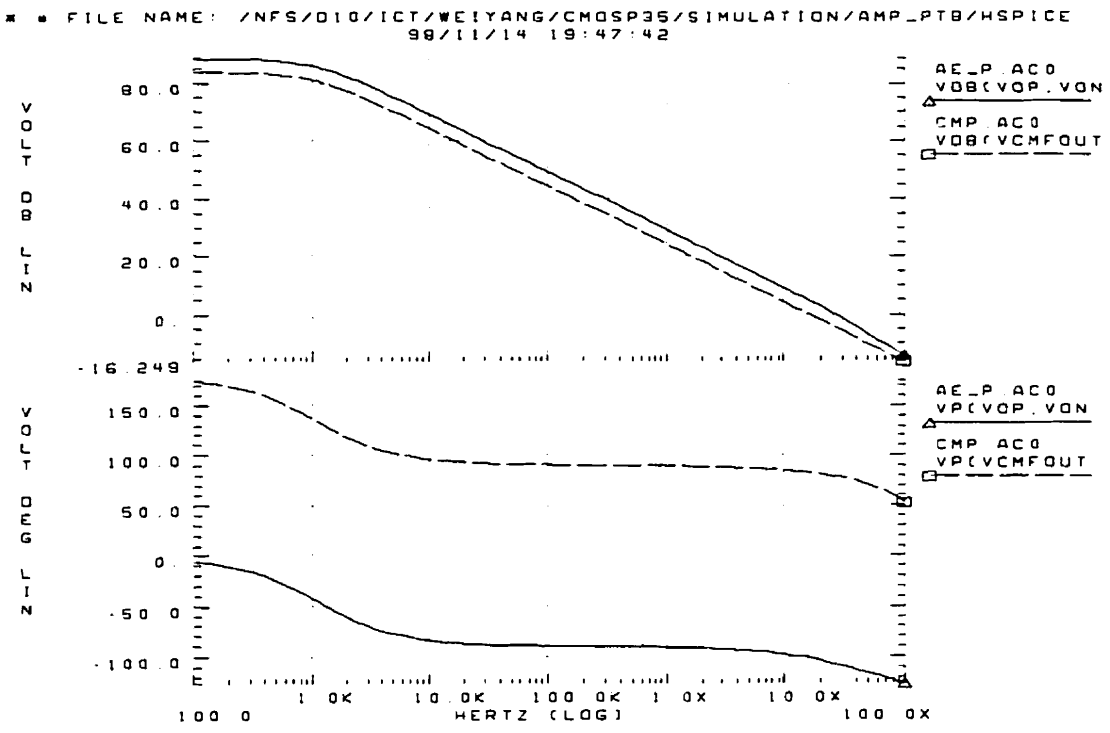

Fig. 3.7: Post-Layout Simulation of Operational Amplifier

The common-mode feedback stage is well compensated with a phase margin of 82 degrees. This is necessary otherwise the injection of common-mode signals can cause the circuit to ring and become unstable. It also has a speed-performance comparable to the unity-gain frequency of the differential stage, otherwise the noise on the power supplies may be significantly amplified such that the output signal becomes clipped [1]. In this design, since the common-mode path actually shares the same dominant pole and the second pole with the differential path, as illustrated in Figure 3.7, the frequency response of both paths are comparable to each other.

3.3 Comparator-Latch

The comparator-latch determines the output of the second integrator and generates either a "one" or a "zero" digital signal within half a clock period. These digital signals are

the modulator's final outputs, and are also used to control the reference voltages of the switched-capacitor feedback loop [2].

3.3.1 Architecture

The fully symmetrical schematic design of the comparator-latch is shown in Figure 3.8 [3, 4]. Vinp and Vinn are the analog inputs. Qp and Qn are the digital outputs.

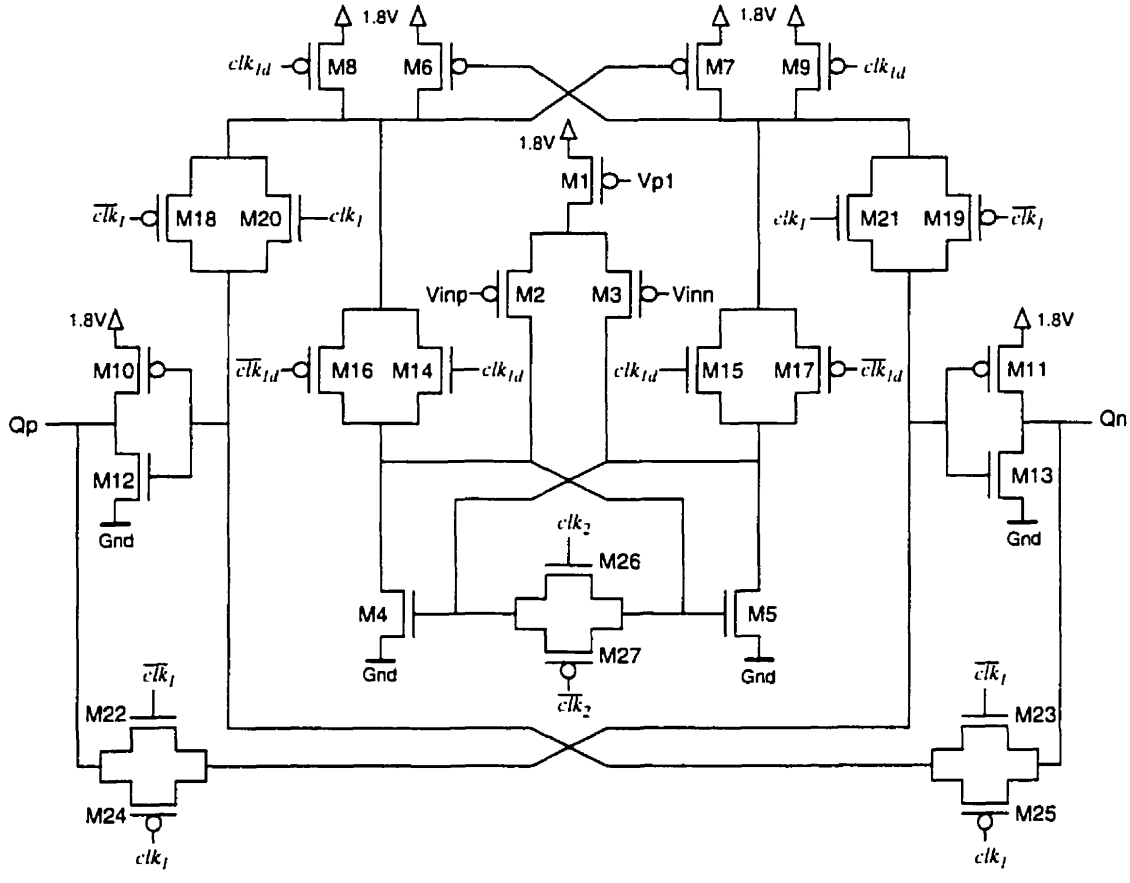

Fig. 3.8: Schematic Design of Comparator-Latch

M1 to M3 make up the input differential pair. M4 and M5 make up an n-channel flip-flop with a pair of CMOS transmission gates (M14 to M17) for strobing, and a CMOS transmission gate (M26 and M27) for resetting. M6 and M7 make up a p-channel flip-flop with two p-channel reset transistors (M8 and M9). M10 to M13 make up a latch that is composed of two back-to-back inverters connected by two pairs of CMOS transmission

gates (M18 to M25) [2, 5]. The comparator-latch is driven by the clock signals generated by the clock generator.

The differential errors caused by the charge injection from transistors M14 to M17, the mismatch in the p-channel flip-flop, the two precharge transistors (M4 and M5), and the latch circuit are divided by the amplification gain when referred to the input as an equivalent offset voltage. Their contribution to the total equivalent input offset voltage can be neglected if the gain is large enough. The size choice of transistors M4 and M5 is important. It is a trade off between mismatch and speed. The on-resistance generated by the transmission gate composed by M26 and M27 must be small enough to pull back the voltages on the drains of M4 and M5 during the reset period so as to eliminate the hysteresis and offset effects. However, these offset and noise errors are really not crucial because they are suppressed by the feedback loop of the modulator since the additive noise undergoes the same spectral shaping as the quantizing noise [6].

The comparator-latch's operation modes are described in Table 3.6, with respect to the different clock states as shown in Figure 3.9. The component values of the comparator-latch are list in Table 3.7. To achieve a high comparison speed, the minimum channel length is used for all gate transistors.

Table 3.6: Comparator-Latch Operation Modes

	State 1	State 2	State 3	State 4	State 5
clk_1	Low	Low	High	Low	Low
clk_{1d}	Low	Low	High	High	Low
clk_2	High	Low	Low	Low	Low
M4, M5	Reset	Track	Compare	Compare	Track
M6, M7	Reset	Reset	Compare	Compare	Reset
M10 to M13	Store	Store	Compare	Latch	Store

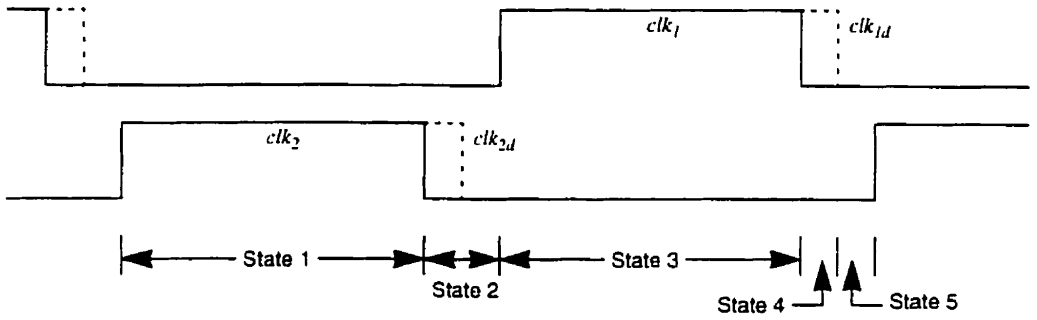

Fig. 3.9: 4-Phase Clock Signals

Table 3.7: Comparator-Latch Component Values

Component	W/L (μm/μm)	Component	W/L (μm/μm)
M1	18/0.7	M16 to M19	6/0.35
M2, M3	14/0.7	M20 to M23	2/0.35
M4, M5	3/0.7	M24, M25	6/0.35
M6 to M11	6/0.35	M26	4/0.35
M12 toM15	2/0.35	M27	10/0.35

3.3.2 Layout

Figure 3.10 is the layout of the comparator-latch.

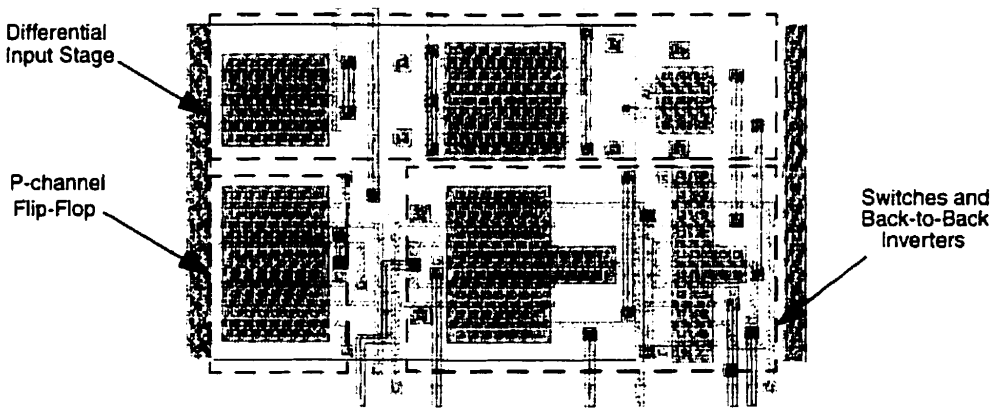

Fig. 3.10: Comparator-Latch Layout

The upper half part is the differential input stage. The P-channel flip-flop is on the lower left hand side of the layout, while the CMOS switches and the back-to-back inverters are on the lower right hand side of the layout. The total comparator-latch layout area is 38X25 μm^2.

3.3.3 Simulation Results

Figure 3.11 shows the post-layout simulation of the comparator-latch. On the top are the two-phase differential input signals. In the middle is the 2.56 MHz clock signal. On the bottom is the comparator-latch output. The comparator-latch works well with the differential voltage as low as 0.12 V. The non-overlapping period between the falling edges of clk_1 and clk_2 is chosen to be 5 ns. The total delay of the comparator-latch is roughly 1.3 ns.

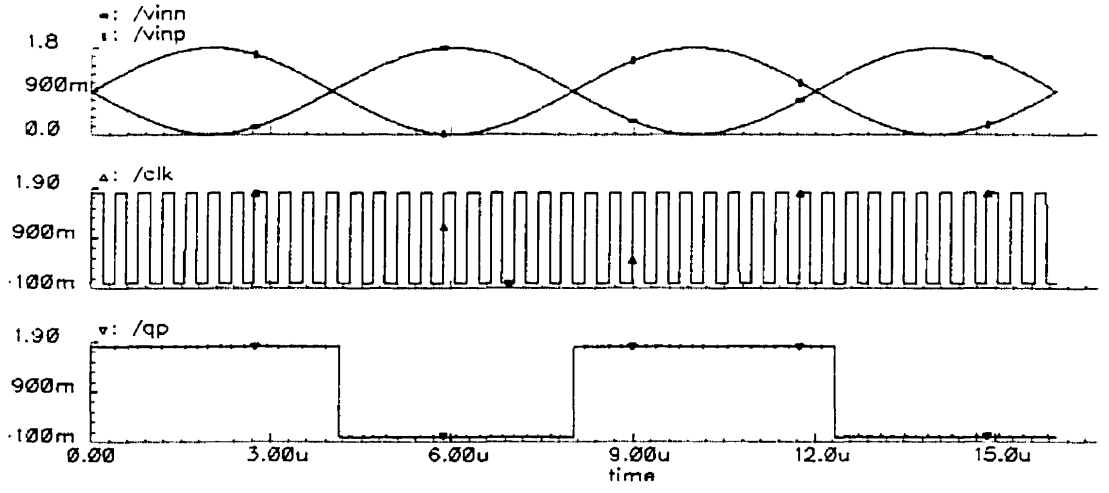

Fig. 3.11: Post-Layout Simulation of Comparator-Latch

3.4 Clock Generator

With a single square wave clock signal as the input, the clock generator provides eight output clock signals for the operational amplifier, the comparator-latch, and the switched-capacitor network of the entire modulator.

3.4.1 Architecture

Figure 3.12 is the schematic of the clock generator which is comprised of several inverters and nand-gates.

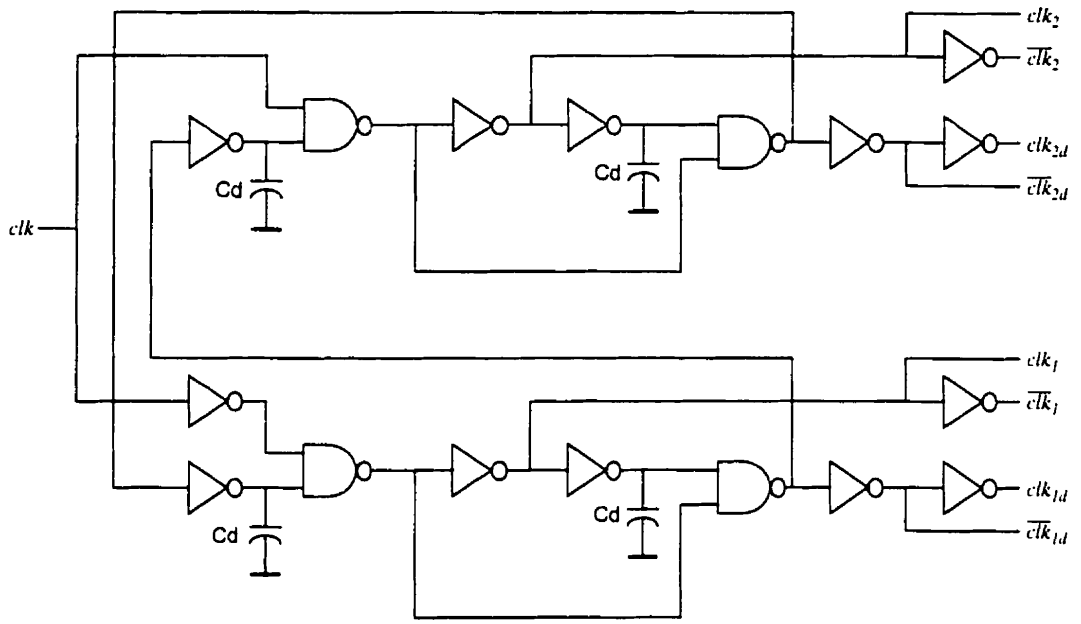

Fig. 3.12: Schematic of Clock Generator

Four capacitors labelled Cd are used to generate the delayed-version clock signals. *clk* is the input clock signal. clk_1 and clk_2 are the two non-overlapping clock signals, while clk_{1d} and clk_{2d} are the delayed versions that have the same raising edge as clk_1 and clk_2, but a delayed falling edge. The counter pulse of every clock is also generated so as to drive the transmission gates in the modulator. The relationship of the four-phase clock signals is shown in Figure 3.9.

3.4.2 Layout

Figure 3.13 shows the layout of the clock generator. The large squares on the right side are the delaying capacitors, while on the left are the gate transistors. The total area of the clock generator is 270X130 μm^2, while the capacitors occupy the area of 230X130 μm^2.

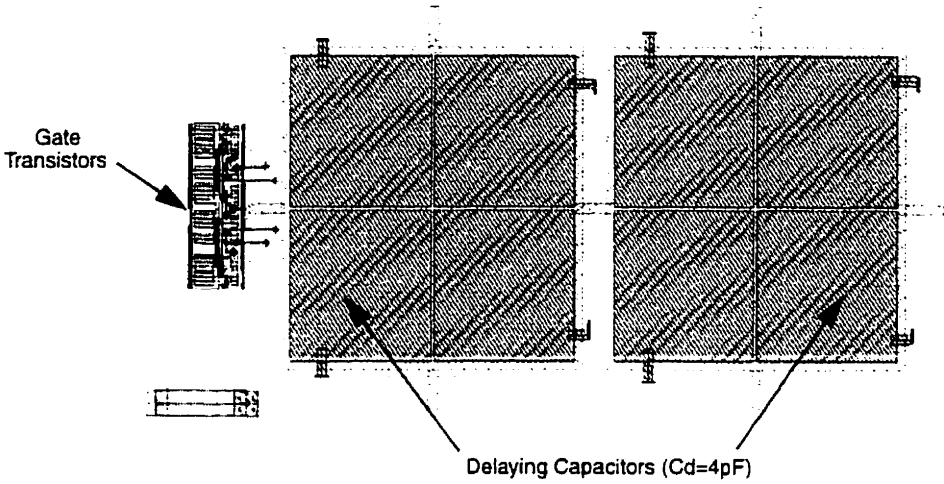

Fig. 3.13: Clock Generator Layout

3.4.3 Simulation Results

Post-layout simulation of the clock generator was performed with the input clock frequency 2.56 MHz, as shown in Figure 3.14.

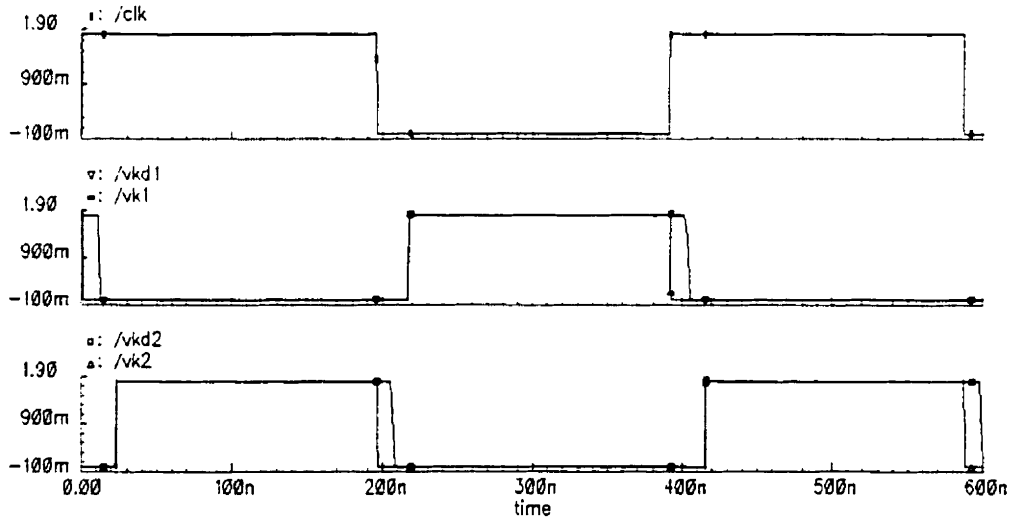

Fig. 3.14: Clock Generator Post-Layout Simulation

When capacitors Cd are chosen to be 4 pF, the non-overlapping period equals 10 ns which is much larger than the minimum requirement of comparator-latch (5 ns). Since the

common-mode feedback circuit, the comparator-latch and the switched-capacitor network of the modulator need all these clocks to drive, each clock's driving load is different.

3.5 Sigma-Delta Modulator

3.5.1 Architecture

The fully differential switched-capacitor configuration of the second-order ΣΔ modulator implementation is shown in Figure 3.1. Vinp and Vinn are the inputs, Qp and Qn are the outputs. To limit the effect of distortion, the maximum differential input range was chosen to be 1.2 V. With a common-mode voltage of 0.9 V, Vdd and Vss are used as the reference voltages controlled by the comparator output. Two capacitor pairs labelled C2 and C5 were added before the two integrators to realize the proper feedback attenuation. The capacitor values for the switched-capacitor network are shown in Table 3.8.

Table 3.8: Capacitor Values for the Modulator Implementation

Capacitor	C1	C2	C3	C4	C5	C6
Value	2.0 pF	1.33 pF	8.5 pF	1.25 pF	0.34 pF	3.0 pF

Operation of the modulator is controlled by the non-overlapping clock signals generated by the clock generator. The switches near the virtual ground nodes of the operational amplifiers are turned off first to reduce the charge injection effects, minimize distortion and gain error and keep the DC offset low [1]. All the switches connected to the inputs of the operational amplifier were realized by single NMOS transistors while the others were realized by CMOS transmission gates.

3.5.2 Experimental Implementation

The die micrograph of the second-order ΣΔ modulator implementation using the double-poly, 0.35μm CMOS process is illustrated in Figure 3.15. It consists of an entire modulator and an opamp test circuit.

On the left is the modulator. The upper part consists of the two operational amplifiers used for integration, between which lies the bias circuit. Immediately below them are the integrating capacitors. On the right corner below them is the comparator-latch protected by a guard ring. The clock generator and the switches, which are also surrounded by a guard ring, reside at the bottom.

On the right is the operational amplifier test circuit, which consists of an opamp, a bias circuit, and a clock generator. This part of the circuit is mainly used to specify the proper compensation capacitors to ensure the stability of the opamp in case of processing variations.

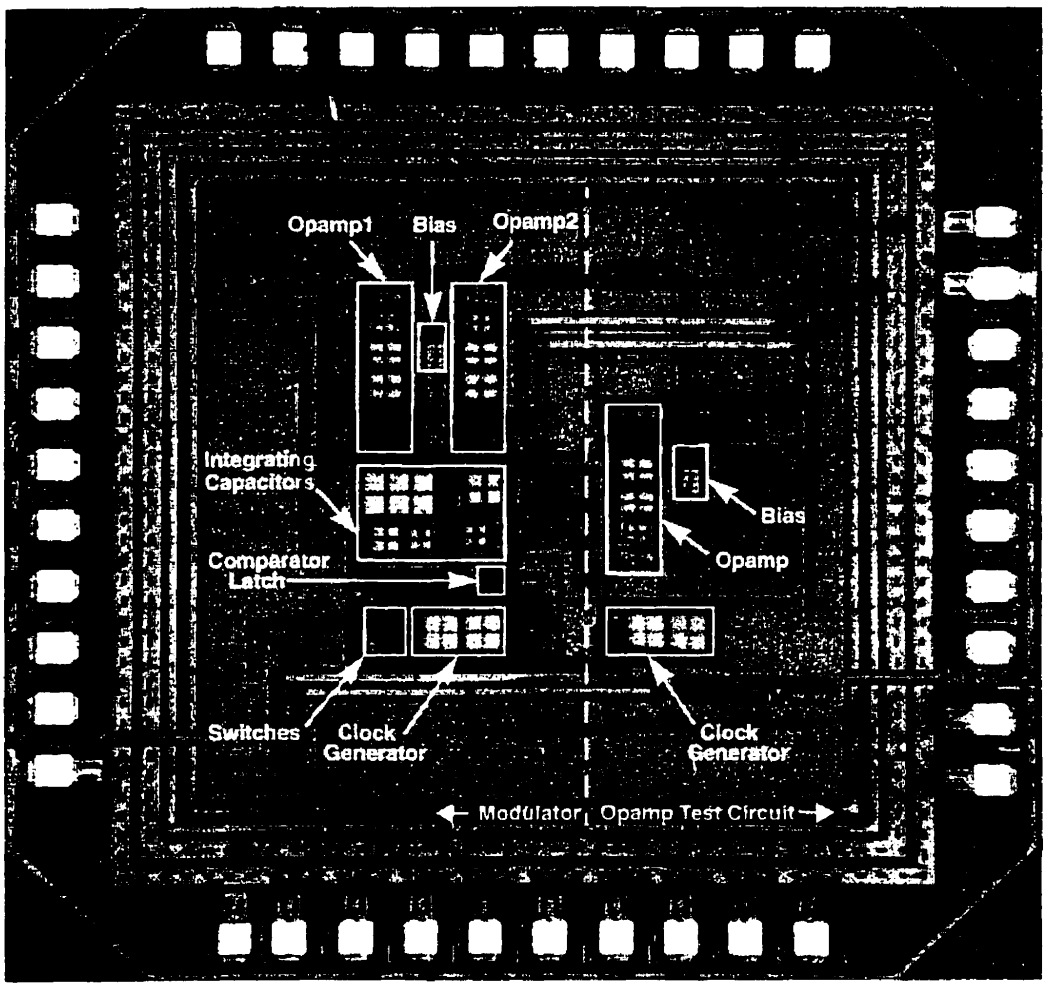

Fig. 3.15: Die Micrograph of the 2nd-order ΣΔ Modulator Implementation

To reduce balancing errors due to processing and temperature variations across the chip, as well as noise induced from transient substrate currents, every pair of components in the balanced signal path (including transmission gates, transistors, and switched capacitors) were arranged in a common-centroid fashion [1, 7]. Wiring runs were also matched because of the parasitic capacitances [6].

Care was also taken in the layout of the capacitor to prevent degradation of the *SNR*, which is sensitive to mismatches occurring in switched capacitors [8-11]. All the capacitors were placed in N-wells biased to the analog ground, thereby reducing the substrate noise and the coupling between the capacitors [12]. Because the bottom plate of a capacitor has a large parasitic capacitance between it and ground, the input side of an amplify stage was always connected to the top plate.

Different circuit blocks such as analog circuits, transmission gates, digital logic circuits were powered from their respective on-chip power and ground wiring so as to reduce the common-mode induced crosstalk.

The area of the entire design including 40 I/O pads is 2550X2590 μm^2. The core modulator area is 310X1000 μm^2.

3.6 Modulator IC Chip Test

3.6.1 Bias Circuit

The measured output voltages of the bias circuit are listed in Table 3.9. The off-chip bias resistance was adjusted to achieve the proper bias voltages. Compared with the results listed in Table 3.2, the experimental and simulation values agree within 6%.

Table 3.9: Measured Outputs of Bias Circuit (Vdd=1.8V)

Parameter	Vn1	Vn2	Vp1	Vp2	Rb
Value	0.867 V	1.240 V	0.856 V	0.376 V	8.4 kΩ

3.6.2 Clock Generator

All the clock signals were tested. As an example, Figure 3.16 shows the measured relationship between clk_1 and clk_2. The measured non-overlapping period is 12 ns, a little bit larger than simulated. The measured rise time t_r is 7 ns, and fall time t_f is 3 ns.

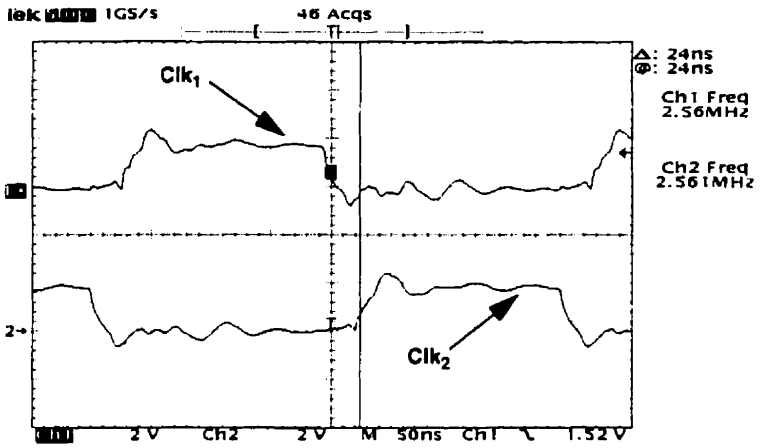

Fig. 3.16: Measured clk_1 and clk_2 Clock Signals

3.6.3 Operational Amplifier

The performance of the fully-differential amplifier was tested by using an inverting configuration with negative feedback as shown in Figure 3.17. Vin and Vip are the differential inputs. Von and Vop are the differential outputs.

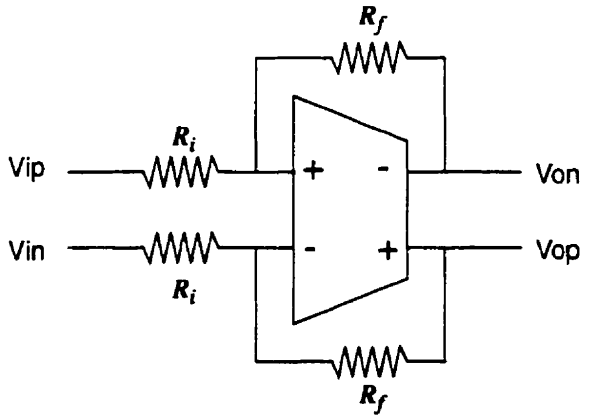

Fig. 3.17: Inverting Amplifier Configuration

The comparison between measurement and simulation results is shown in Figure 3.18. The measured gain-frequency product is 21 MHz, which is slightly smaller than the simulation result (25 MHz). The open-loop DC gain was estimated to be 87 dB, which is very close to the simulated (89 dB).

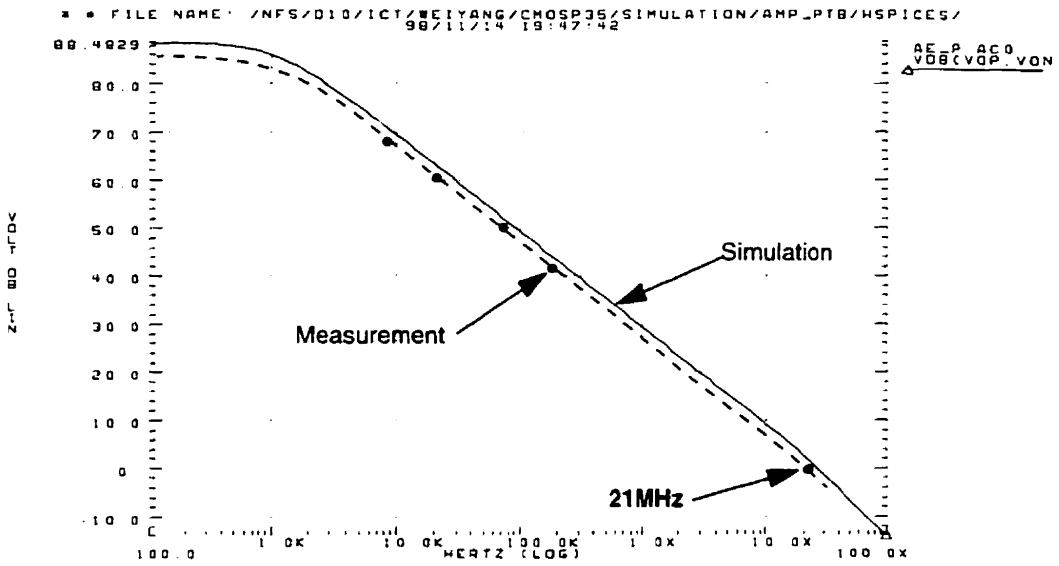

Fig. 3.18: Gain Performance of Operational Amplifier

The operational amplifier was set up to be in the unity-gain configuration to measure the slew rate and the phase margin. Without a 16 .7pF parasitic capacitance (measured using HP4284A Precision LCR Meter) on the PCB test board, with a 2.3 pF compensation capacitance, the operational amplifier exhibited a slew rate of 28 V/μs, and a phase margin of 68 degree, which were very close to the simulation results (31 V/μs slew rate, 73 degree phase margin).

3.6.4 Modulator Performance

With the proper bias voltages and the well-compensated integrators, a fully differential 1kHz sinusoidal signal with the common-mode voltage around 0.9 V was used to drive the modulator inputs. Figure 3.19 shows that, with a 1.2 Vpp input signal amplitude, and a 200 kHz sampling frequency, the output digital pulse is correctly pulse-density modulated.

With a 2.56 MHz sampling frequency, Figure 3.20 shows that, after a decoder is applied on the modulator's digital output, the input signal is reconstructed successfully.

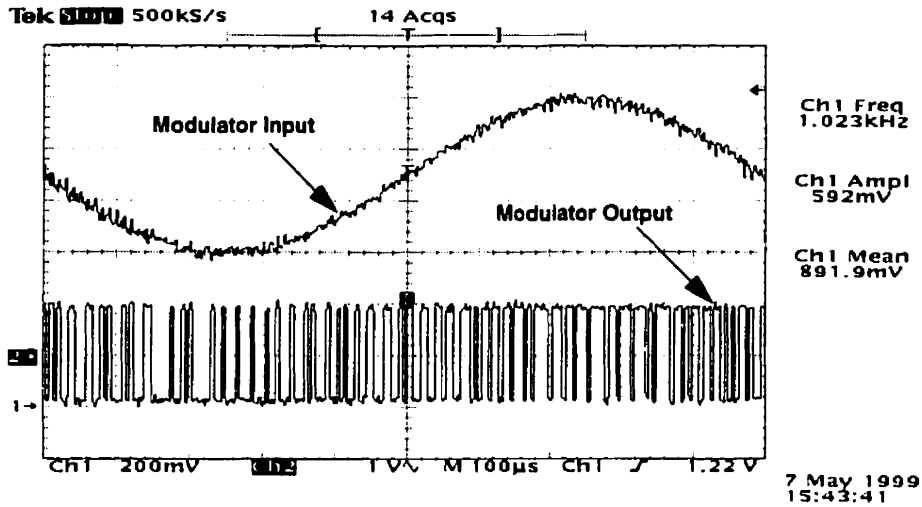

Fig. 3.19: Measured Pulse-Density-Modulated Modulator Output

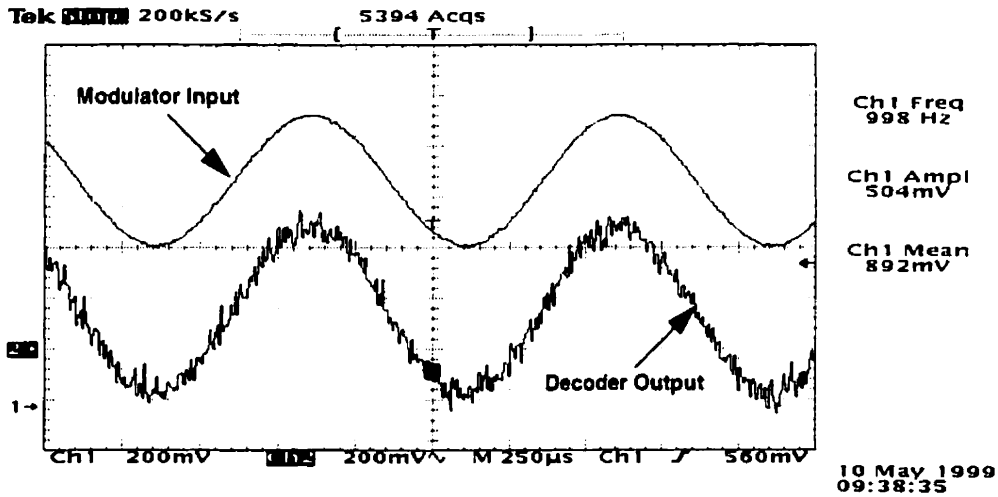

Fig. 3.20: Reconstructed Input Signal from the Measured Modulator Output

The digital output of the modulator was acquired and stored on a computer. A dedicated C-program and Matlab were used for the subsequent signal processing. Figure 3.21 shows the full spectrum calculated from the measured output data with an input normalized level of -74 dB, a sampling frequency of 2.56 MHz, and an input signal frequency of 1 kHz.

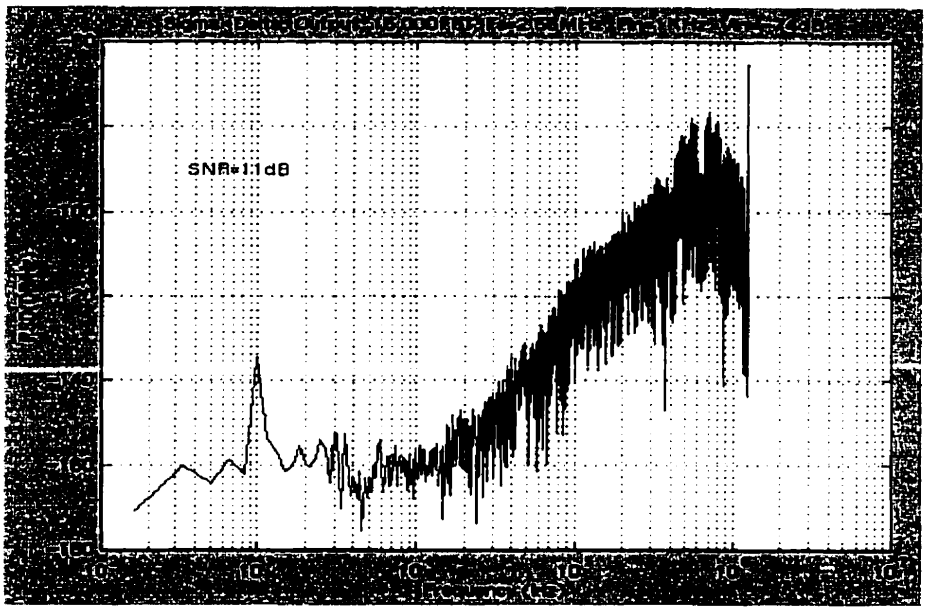

Fig. 3.21: Full Spectrum of the Measured Modulator Output

The modulator achieves 11 dB of *SNR* in 7 kHz signal bandwidth with the desired over-sampling and noise-shaping. The noise floor level is as low as -160 dB. A large amount of output data was sampled and calculated with various input signal levels. The measured *SNR* and *SNDR* versus normalized input level is shown in Figure 3.22.

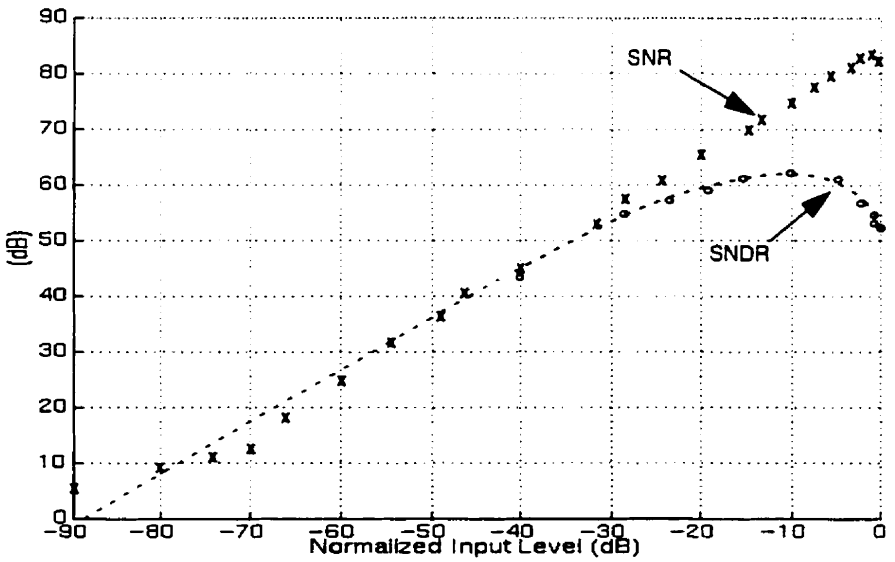

Fig. 3.22: Measured *SNR* and *SNDR* versus Normalized Input Level

The modulator achieves 15-bit dynamic range and a peak *SNR* of 85 dB with a 7 kHz bandwidth. For a 20 kHz bandwidth, the dynamic range is 14 bits with a peak *SNR* of 78 dB. The input full-scale range was designed to be 1.2 V. Test results show that it can be extended to 1.8 V to provide extra dynamic range compensating for the loss due to the practical worse-than-predicted mismatch and circuit noise. The measured *SNDR* reduces as the signal level increases. The peak *SNDR* reaches 62 dB which is much lower than *peak SNR* because *SNDR* is mainly limited by the second-order harmonic distortion which is usually pronounced especially in low-voltage design.

Table 3.10 summarizes the performance of the 2nd-order ΣΔ modulator. Comparing with Grilo's design, with the same order, the same power supply voltage, and the same sampling frequency range, this design can achieve the same dynamic range, at double the signal bandwidth, and with half the power dissipation, and a smaller die area.

Table 3.10: Measured Performance and Comparison with Previous Design [11]

Specifications	This Design		Grilo [11], 1996
Order of ΣΔ	2nd		2nd
Dynamic Range	15 bits	14 bits	15 bits
Signal Bandwidth	7 kHz	20 kHz	3.5 kHz
Sampling Frequency	2.56 MHz		2 MHz
Input Common-mode Level	0.9 V		1.2 V
Maximum Input Level	1.8 Vpp		1.2 Vpp
Power Supply Voltage	1.8 V		1.8 V
Power Dissipation	0.99 mW		2 mW
Chip Active Area	0.31 mm^2		0.44 mm^2
Technology	0.35μm CMOS		0.6μm CMOS

3.7 Summary

This chapter has dealt with the design and implementation of a low-voltage low-power 2nd-order ΣΔ modulator. The design and layout of all the building blocks were presented and discussed. Post-layout simulations and measured results showed that each block works well with satisfactory performance. The modulator was realized with a fully-differential switched-capacitor configuration and was implemented using a 0.35μm CMOS process. Both functional and performance tests were performed on the modulator IC chip. Measured results revealed that the modulator oversampling at 2.56 MHz has 15-bit dynamic range with a 7 kHz bandwidth, and a 14-bit dynamic range with a 20 kHz bandwidth, while dissipating 0.99 mW of power. The die area is 0.31 mm^2 without I/O pads.

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CHAPTER 4

Conclusions

The second-order ΣΔ modulator constitutes an efficient architecture for implementing high-resolution A/D converters in scaled high-performance integrated circuit technology. This thesis investigated the design and the implementation of a low-power low-voltage second-order ΣΔ modulator for portable communication devices using a double-poly, 0.35μm CMOS process, which is optimized for digital circuits.

The theory of oversampling and noise shaping were presented and illustrated by system-level simulations. Detailed design considerations and analytic results have been used to establish the design criteria for the analog circuit blocks comprising the modulator. Specifically, the integrator linearity has a crucial influence on the performance of the modulator, whereas the ΣΔ modulator imposes only modest demands on the integrator's bandwidth, and is relatively insensitive to the offset and hysteresis in the comparator.

The fully-differential operational amplifier is the most important component, which mainly limits the performance of the ΣΔ modulator's performance. The finite DC gain limits the modulator's dynamic range, while the frequency characteristics determines the maximum oversampling ratio. In a low-voltage environment, the voltage swing must be maximized to ensure a large dynamic range. This implies a folded-cascode architecture followed by a common-source output stage, and coupled with a switched-capacitor common-mode feedback stage. The designed operational amplifier can achieve a DC gain

of 87 dB, a phase margin of 68 degree, a slew rate of 28 V/μs, and a unity-gain frequency of 21 MHz.

The modulator consists of four building blocks: the biasing, the operational amplifier, the comparator-latch, and the clock generator. It was designed, implemented and tested. Test results show that each component as well as the final modulator work as expected. With a single 1.8 V supply voltage, the modulator can achieve 15-bit dynamic range with a 7 kHz signal bandwidth and a 2.56 MHz sampling frequency, while dissipating 0.99 mW of power and occupying 0.31 mm^2 of die area. The oversampling ratio is 160.

One advantage of this design is that all the necessary circuit elements are on a single chip, thus a minimum number of interface pins has been realized. Another advantage is that the input common-mode voltage has been chosen at half of the power-supply voltage, thus increasing the circuit compatibility and flexibility.

Several techniques can be tried in future work to further improve the modulator's performance. Reducing the on-resistance of the switches can make the second-order harmonic distortion smaller, thus increasing the peak *SNDR*. Correlated-double-sampling topology can reduce the DC offset and 1 / f noise level, and allow an increase in the sampling frequency without requiring a faster operational amplifier. Relaxing the performance of the second integrator will not impair the modulator performance, and the common-mode feedback stage can be omitted in that case, thus reducing the power dissipation and die area. Furthermore, using a programmable switched-capacitor network can make the modulator meet different practical application standards.

APPENDIX

Modulator IC Chip Test

The purpose of the test is to verify the functionality of the second-order sigma-delta modulator and to characterize its performance: dynamic range, *SNR* and *SNDR*, and power dissipation.

A.1 Test Topology

Basically there are three alternatives for measuring the performance of a ΣΔ modulator. The first one is to feed the 1-bit modulator output into a precise 1-bit D/A converter and then feed this analog output into a spectrum analyzer to measure the noise and distortion. This method is often used when both A/D and D/A are designed on one chip. The disadvantage is that it is difficult to assign any design nonidealities to the A/D converter alone, since the signal is influenced by the performance of the D/A converter as well.

The second method is to digitally filter and decimate the modulator output in hardware to the Nyquist rate, capture that data through a computer interface, and then spectrally analyze the data in software. This approach is advantageous when the desired digital decimation filter is known ahead of time and already exists in hardware. The disadvantage is that one may wish to examine how the analog modulator performs with a different digital decimation filter for some other applications. If that decimation filter does not exist in hardware, then one would have to reply only on simulation.

The third approach is to capture the 1-bit modulator output directly by the computer interface, digitally filter and decimate the modulator data in software, and examine the power spectrum of that data. It has the advantage that the noise and distortion can be determined without any effects from the decimation filter. And if a different digital decimation filter is desired, one can simply write the software corresponding to that architecture. This method is by far the most thorough and accurate approach, and is used in this thesis.

A.2 Equipment and Setup

The necessary equipment used for evaluating the performance of the modulator include DC power supplies, an Audio-Precision System Two, a real-time digital oscilloscope, a function generator, multimeters, a logic analyzer, and a personal computer. The test setup is shown in Figure A.1.

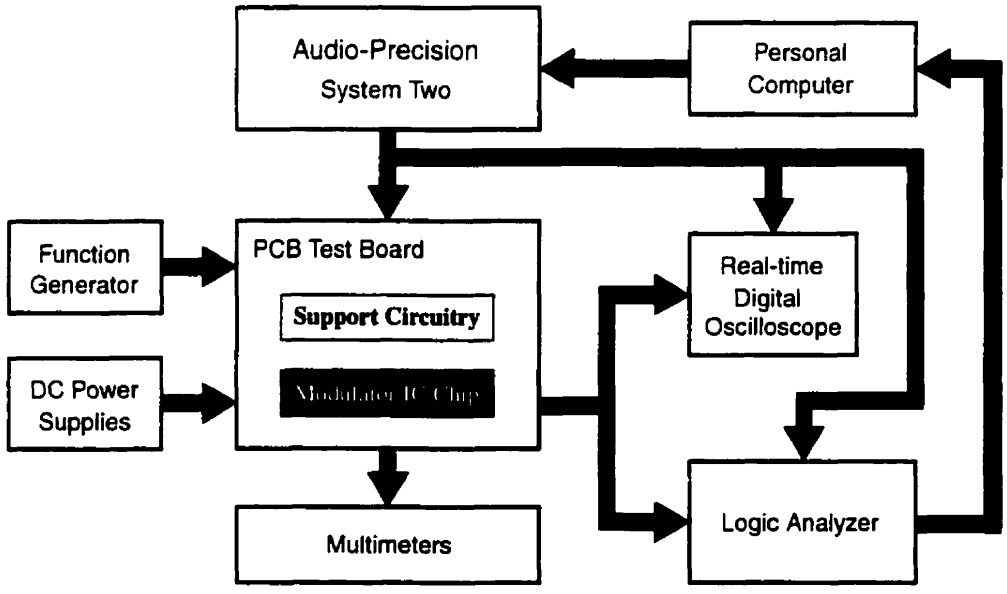

Fig. A.1: Test Setup for ΣΔ Modulator IC

The DC power supplies provide the analog power, the digital power, and the offset voltages for both the modulator and support circuitry. The Audio-Precision System Two provides a differential input signal for the modulator. The real-time digital oscilloscope is used to characterize the driving clock signals generated by the clock generator, to test the operation of the operational amplifier, and to monitor the modulator input and output waveforms. The function generator provides the digital clock input signal. The multimeters are used to measure and monitor both the on-chip and off-chip bias voltages. The logic analyzer serves as a computer interface which is capable of acquiring the modulator's digital outputs and storing them on a harddisk as a file. The personal computer controls the Audio-Precision System Two and executes a C-program for subsequent data processing. The modulator IC chip is placed on the test board which will be described in the following section.

A.3 Test Board

A PCB test board which houses the second-order ΣΔ modulator and the support circuitry has been designed and built with the functional blocks shown in Figure A.2.

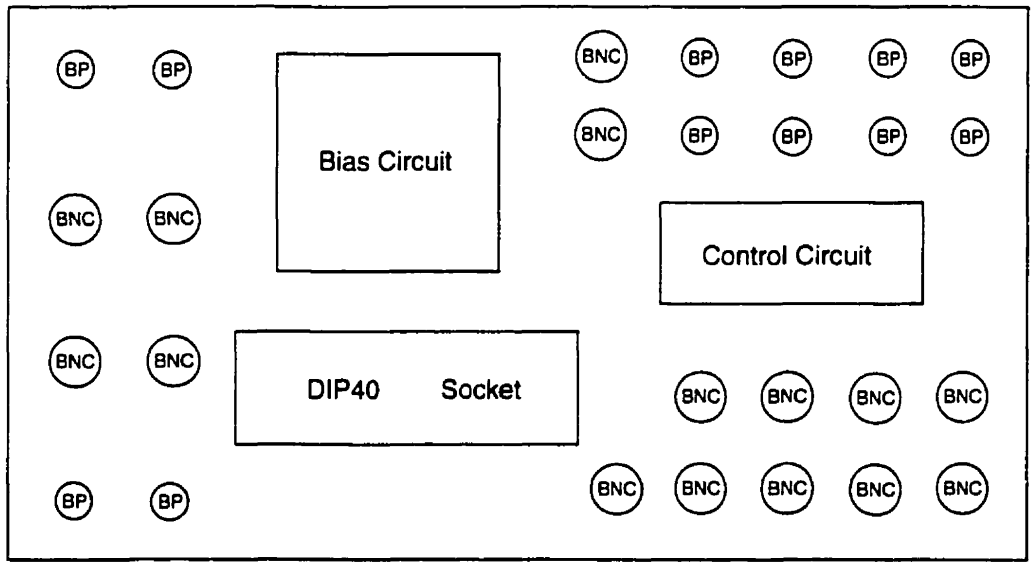

Fig. A.2: PCB Test Board for the Sigma-Delta Modulator

The DIP40 socket holds the second-order ΣΔ modulator IC chip. The bias circuit provides the off-chip bias voltages for the modulator in case the on-chip bias circuit does not work properly due to the process variations. This bias circuit is necessary especially in a low-voltage design. The control circuit set the bias levels and the compensation capacitor values for the operational amplifier. The BNC connectors are used to connect the input and output analog/digital signals of the chip. The BP (binding post) connectors are used to connect the power supply, and to monitor the bias voltages.

A.4 Test procedure

A.4.1 Bias Circuit Test

By adjusting the off-chip resistance, the bias voltages generated by the bias circuit were measured using multimeters.

A.4.2 Clock Signals Test

A 2.56 MHz square wave clock signal, with proper offset voltage, was generated by the function generator and was fed into the modulator's clock input. Using the real-time digital oscilloscope, the eight-phase output clock signals were detected. The phase relationships between them have been checked, and the overlapping period, rise time, and fall time were measured.

A.4.3 Operational Amplifier

The operational amplifier was set up in an inverting amplifier with the negative feedback configuration. A fully-differential sine wave input signal with proper DC offset voltage was generated by the Audio-Precision System Two, and was applied on the amplifier's input. The oscilloscope was used to detect both the input and the output waveforms of the amplifier in order to measure the close-loop gain. Increasing the input

signal frequency up to the point where the output signal amplitude reaches 0.707 times of the original one can find the cut-off frequency of the inverting amplifier. The intercepting points of close-loop gain and cut-off frequency make up the frequency response of the open-loop gain.

Setting the operational amplifier in a unity-gain feedback configuration, a sine input with proper DC offset was applied on the operational amplifier's input. The oscilloscope was used to detect the phase shift between the input and output waveforms to detect the compensation result. With a large amplitude square wave applied on the input, the oparnp output signal was detected, and the slew rate was measured using the oscilloscope.

A.4.4 Characterizing the Modulator

By using the personal computer to control the Audio-Precision System Two, a fully differential sine wave signal with a proper DC offset has been generated and fed into the modulator's input. With the proper on-chip bias voltages and well-compensated integrators, the modulator has been tested functionally by using the oscilloscope to detect the pulse-density-modulated digital outputs.

To evaluate the modulator performance, the original modulator digital output was sampled by the logic analyzer and stored as files on the harddisk of the personal computer. A C-program was created to perform the subsequent data processing. The full spectrum calculations were performed in Matlab. By changing the input signal levels, the corresponding *SNR* and *SNDR* were calculated, and the dynamic range was obtained.